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(54) **DISPLAY DEVICE INCLUDING AN ORGANIC EL DEVICE**

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(60) Continuation of application No. 11/634,089, filed on Dec. 6, 2006, which is a division of application No. 10/304,700, filed on Nov. 27, 2002, now Pat. No. 7,157,847.

(30) **Foreign Application Priority Data**

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(52) **U.S. Cl.** **345/76**

(57) **ABSTRACT**

A self-luminescence display device, in which dispersion in display among a plurality of pixels, caused by dispersion in characteristics among drive thin-film transistors, is decreased and uniform display free of unevenness can be obtained. The device includes a plurality of pixels having current drive type luminescent elements, and parallel-connected n (n≧2) thin-film transistors to feed a drive current to the respective current drive type luminescent elements. The transistors are arranged in different pixels, respectively, for example, in a first region of pixels adjacent to one another along a first direction. A second region of dummy pixels can be provided on at least one side of said first region along said first direction.

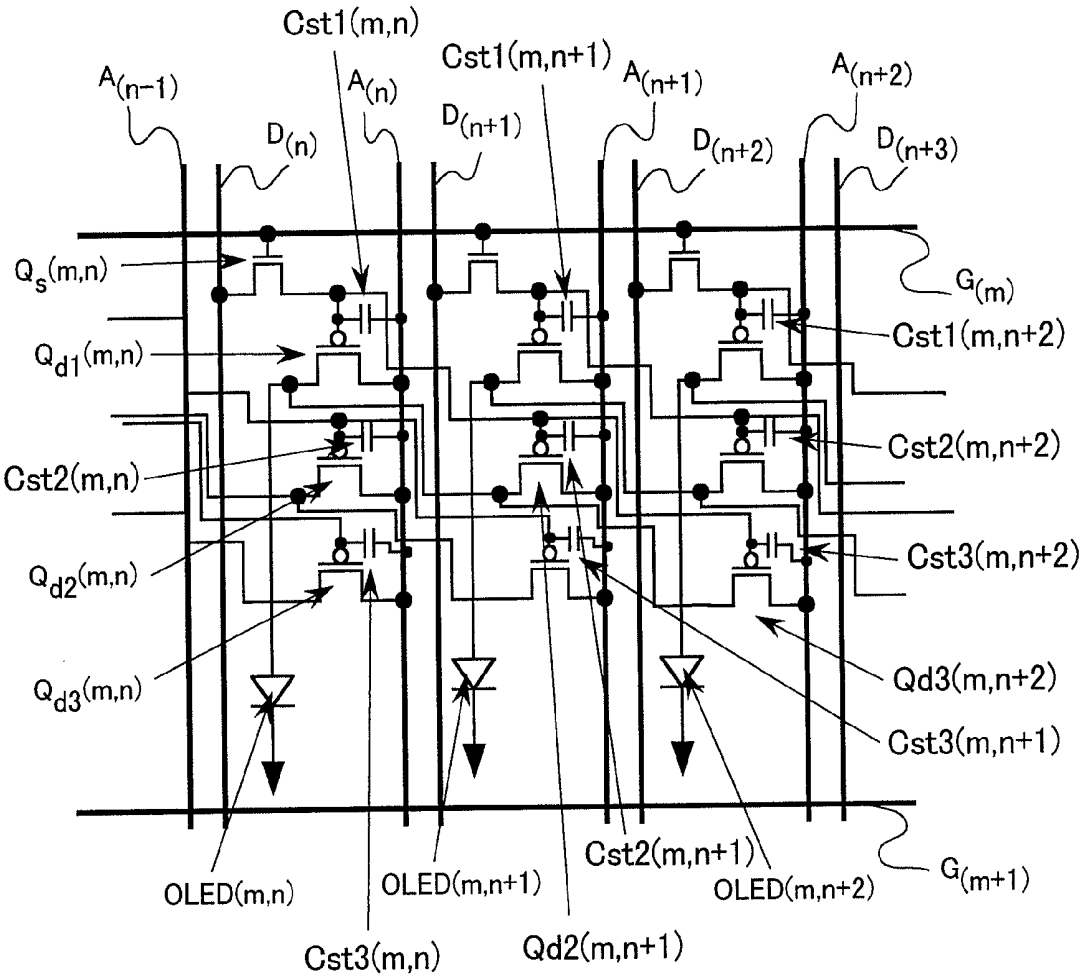


FIG.1

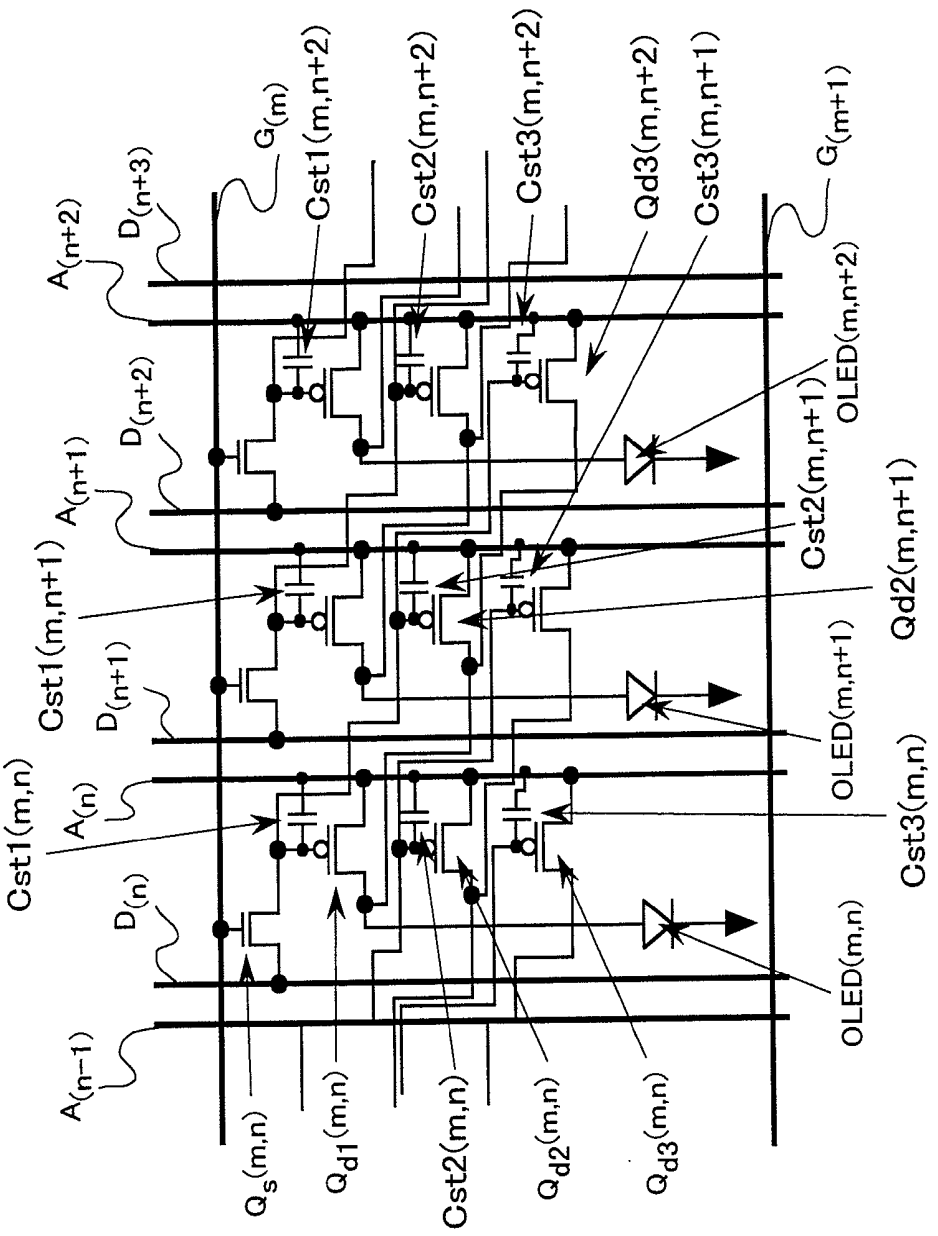

$A_{(n-1)}$
$A_{(n)}$
$A_{(n+1)}$
$A_{(n+2)}$
$D_{(n)}$
$D_{(n+1)}$
$D_{(n+2)}$
$D_{(n+3)}$
$G_{(m)}$
$G_{(m+1)}$
Cst1(m,n)
Cst1(m,n+1)
Cst1(m,n+2)
Cst2(m,n)
Cst2(m,n+1)
Cst2(m,n+2)
Cst3(m,n)
Cst3(m,n+1)
Cst3(m,n+2)
Qd2(m,n+1)
Qd3(m,n+2)
OLED(m,n)
OLED(m,n+1)
OLED(m,n+2)
$Q_s(m,n)$
$Q_{d1}(m,n)$
$Q_{d2}(m,n)$
$Q_{d3}(m,n)$

FIG.2

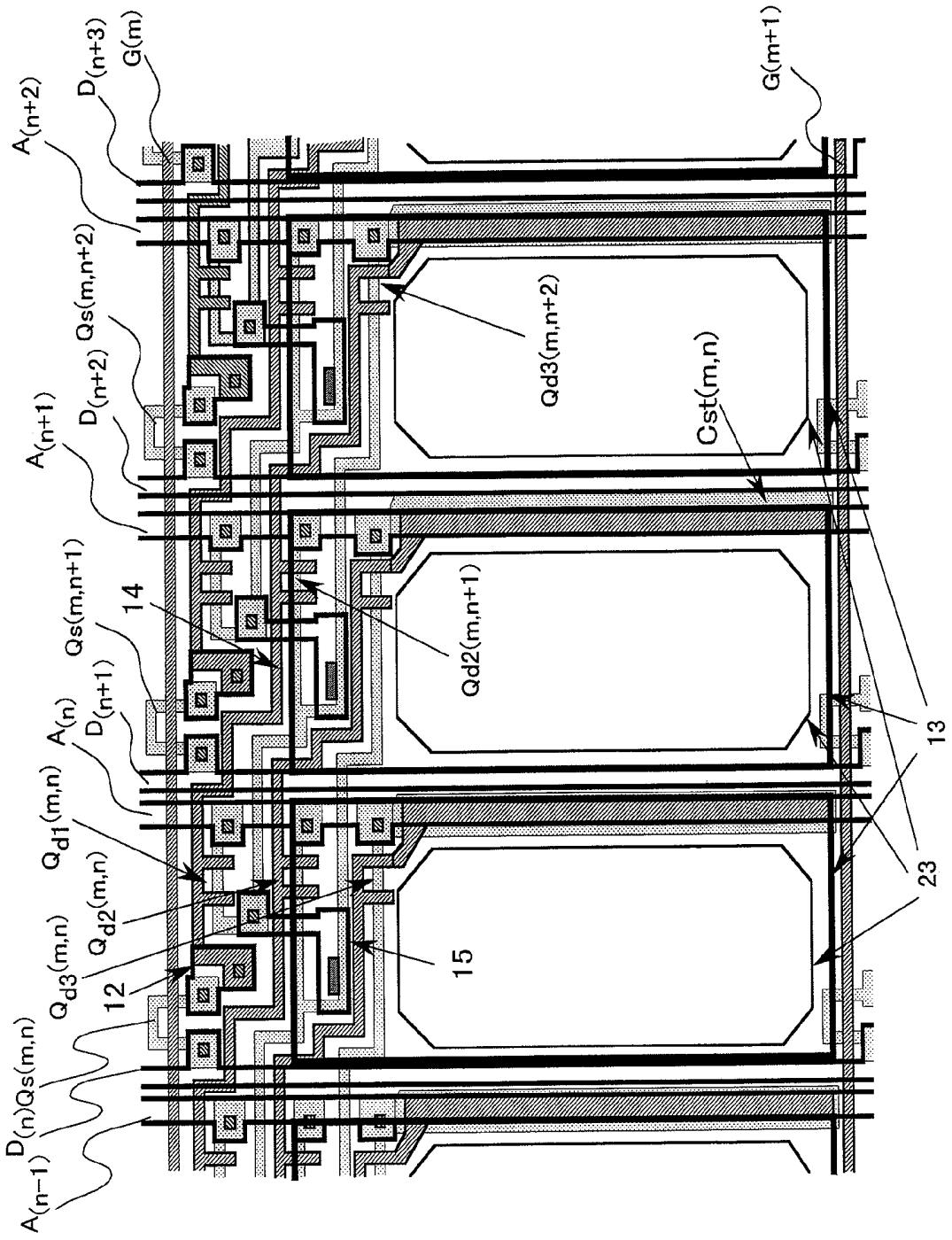

A(n+2)
D(n+3)
G(m)
G(m+1)
Qs(m,n+2)
D(n+2)
A(n+1)
Qs(m,n+1)
14
D(n+1)
A(n)
Qd1(m,n)
Qd2(m,n)
Qd3(m,n)
12
D(n)Qs(m,n)
A(n-1)
Qd3(m,n+2)
Cst(m,n)
Qd2(m,n+1)
15
13
23

FIG.3

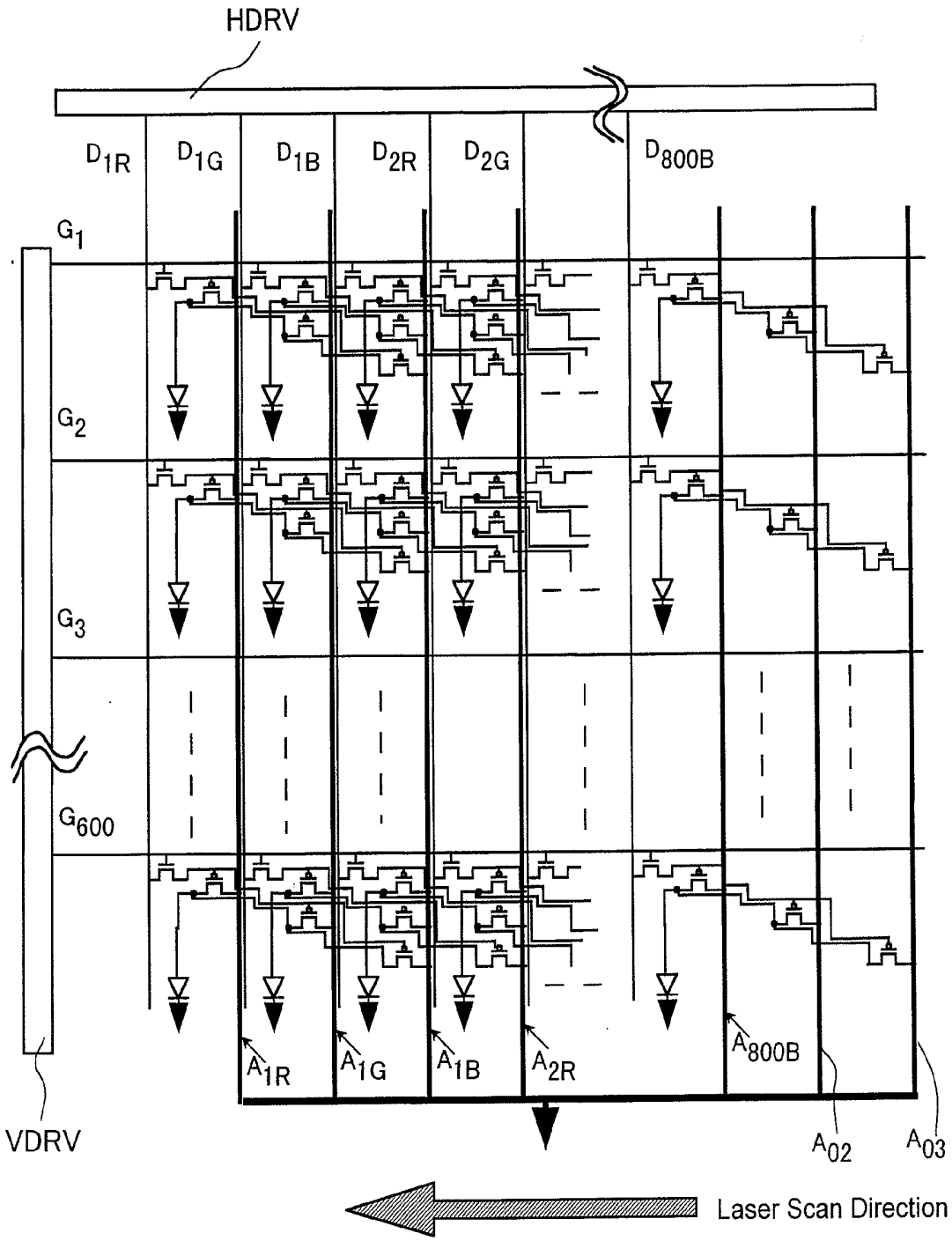

HDRV
D1R
D1G
D1B
D2R
D2G
D800B
G1
G2
G3
G600
A1R
A1G
A1B
A2R
A800B
A02
A03
VDRV
Laser Scan Direction

FIG.4

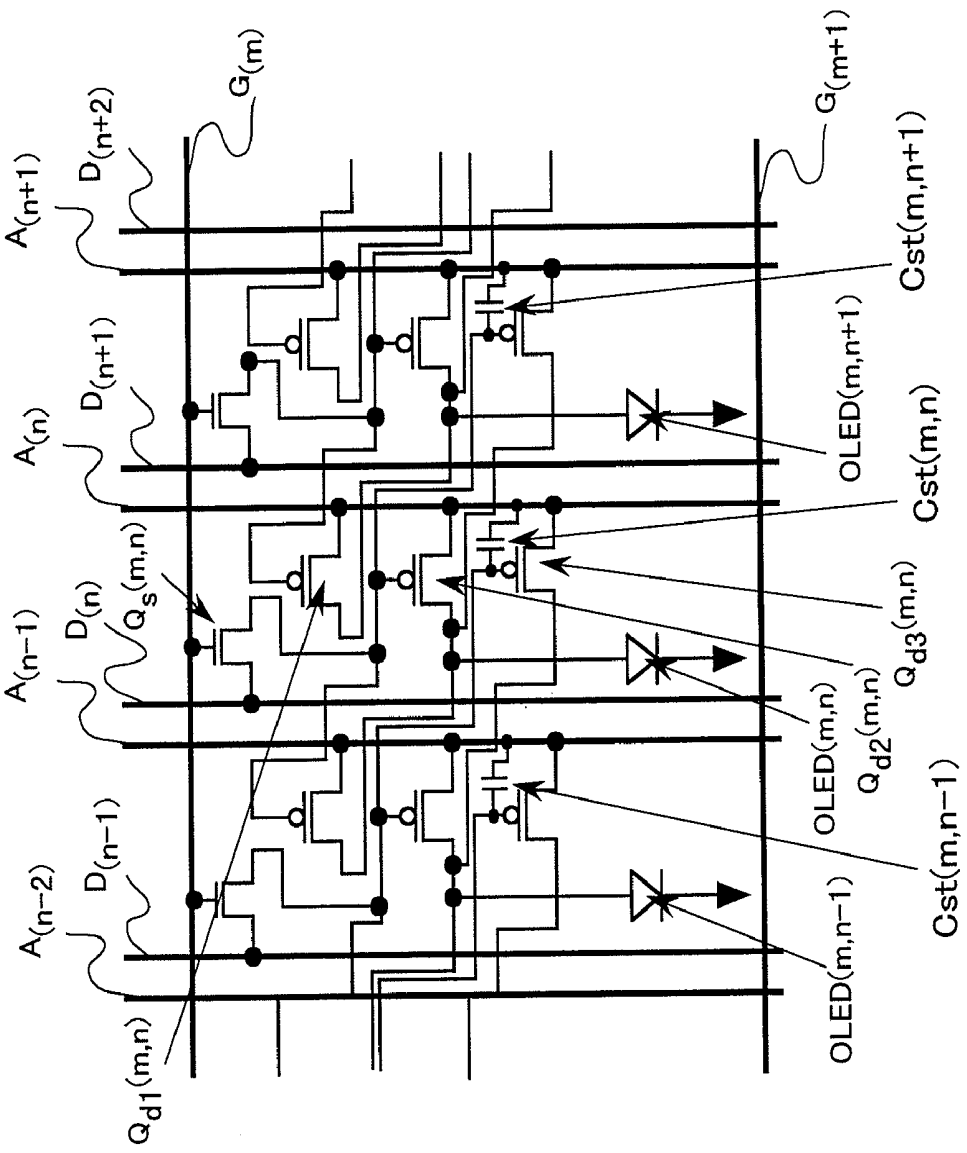

$A_{(n+1)}$
$D_{(n+2)}$
$G_{(m)}$
$G_{(m+1)}$
$A_{(n)}$
$D_{(n+1)}$
$A_{(n-1)}$
$D_{(n)}$
$Q_s(m,n)$
$A_{(n-2)}$
$D_{(n-1)}$
$Q_{d1}(m,n)$
$Cst(m,n+1)$
$OLED(m,n+1)$
$Cst(m,n)$
$Q_{d3}(m,n)$
$OLED(m,n)$
$Q_{d2}(m,n)$
$Cst(m,n-1)$
$OLED(m,n-1)$

FIG.5

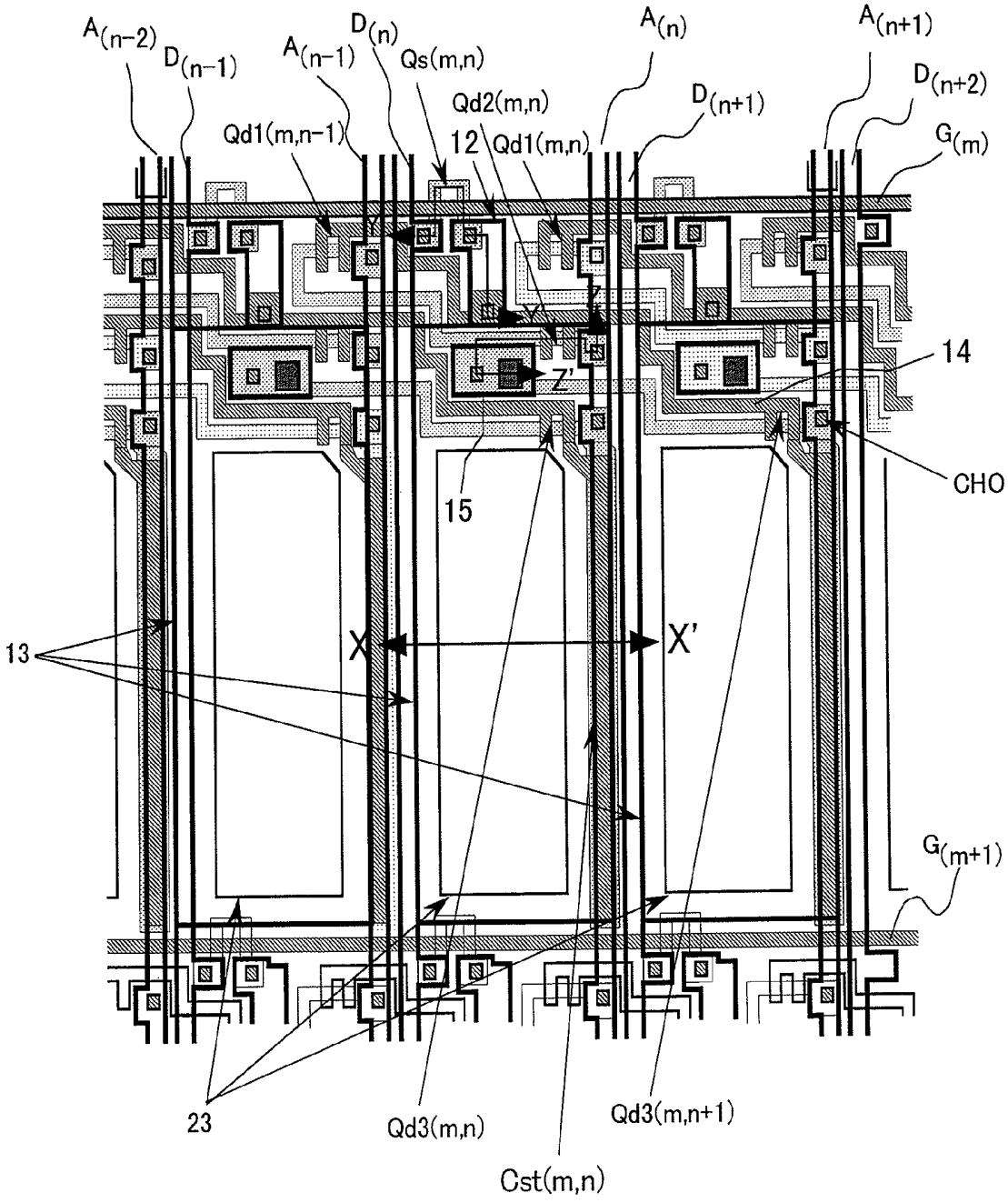

A(n-2)
D(n-1)
A(n-1)
D(n)
Qs(m,n)
A(n)
A(n+1)
D(n+1)
D(n+2)
Qd2(m,n)
Qd1(m,n-1)
12
Qd1(m,n)
G(m)
Y
Y'
Z
Z'
14
15
CHO
13
X
X'
G(m+1)
23
Qd3(m,n)
Qd3(m,n+1)
Cst(m,n)

FIG.6

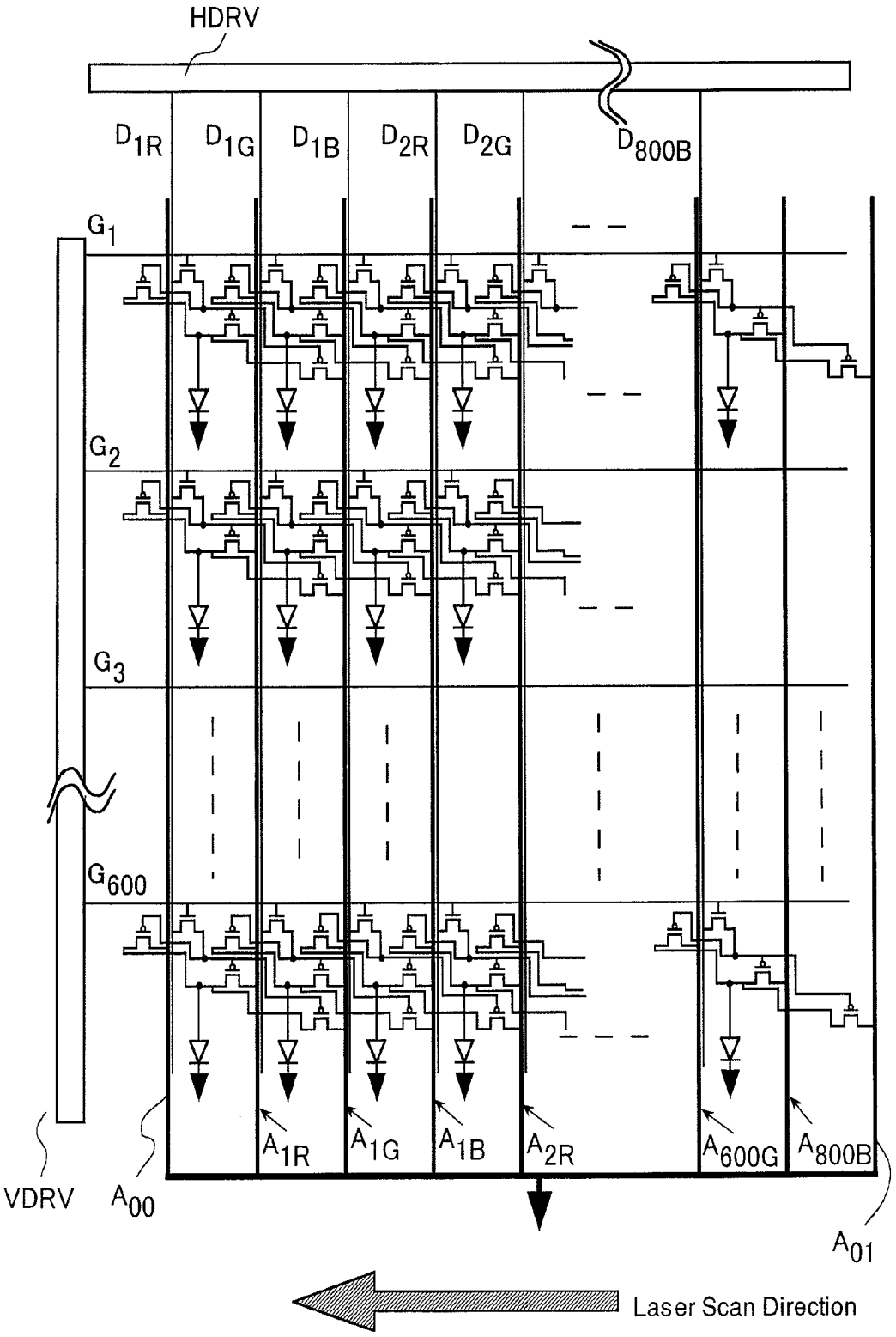

HDRV
D1R
D1G
D1B
D2R
D2G
D800B
G1
G2
G3
G600
VDRV
A00
A1R
A1G
A1B
A2R
A600G
A800B
A01
Laser Scan Direction

FIG.7

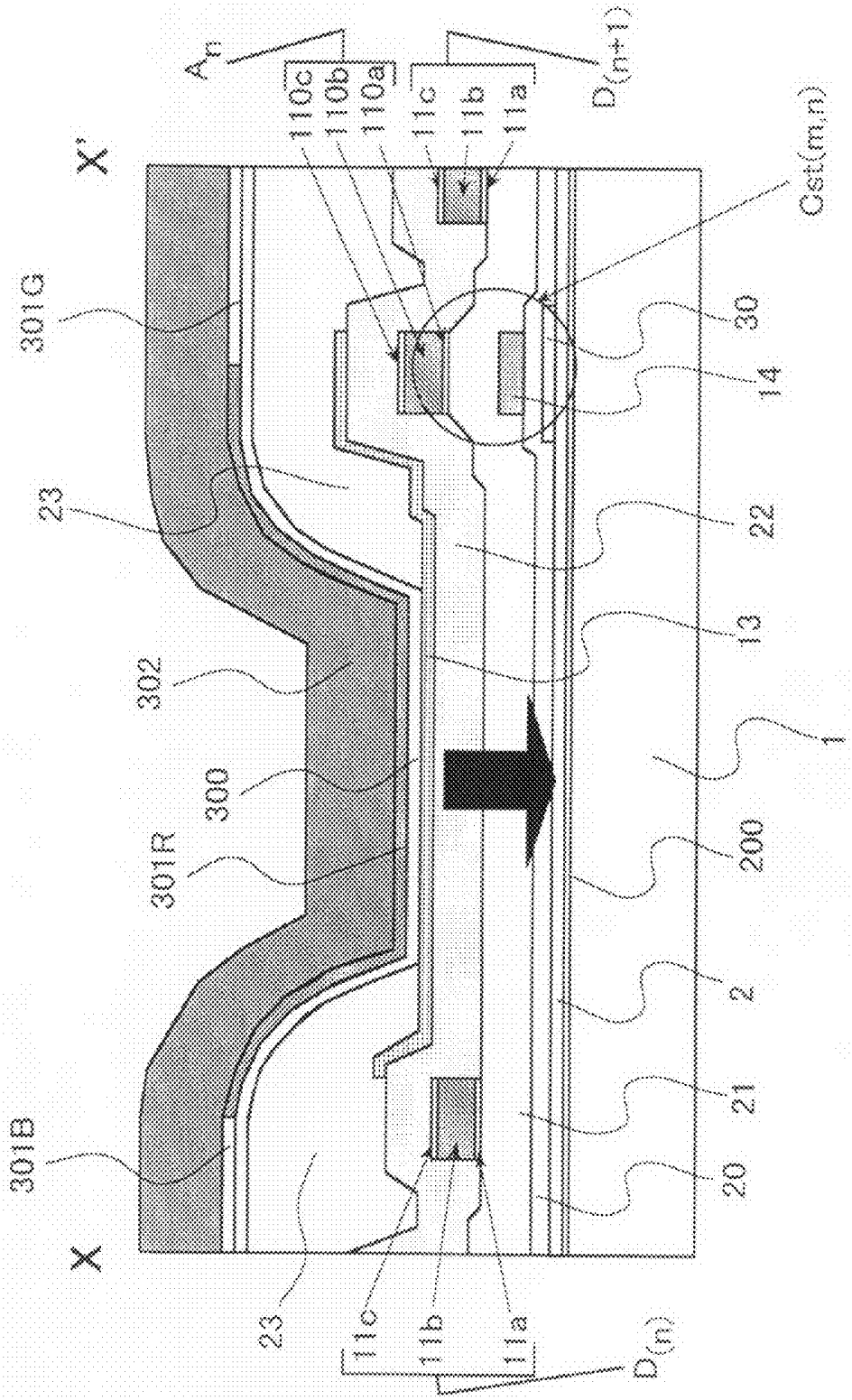

X
X'
301B
301R
300
302
301G
23
20
21
2
200
1
13
22
14
30
Ost(m,n)
D(n)
D(n+1)
11a
11b
11c
110a
110b
110c

FIG.8

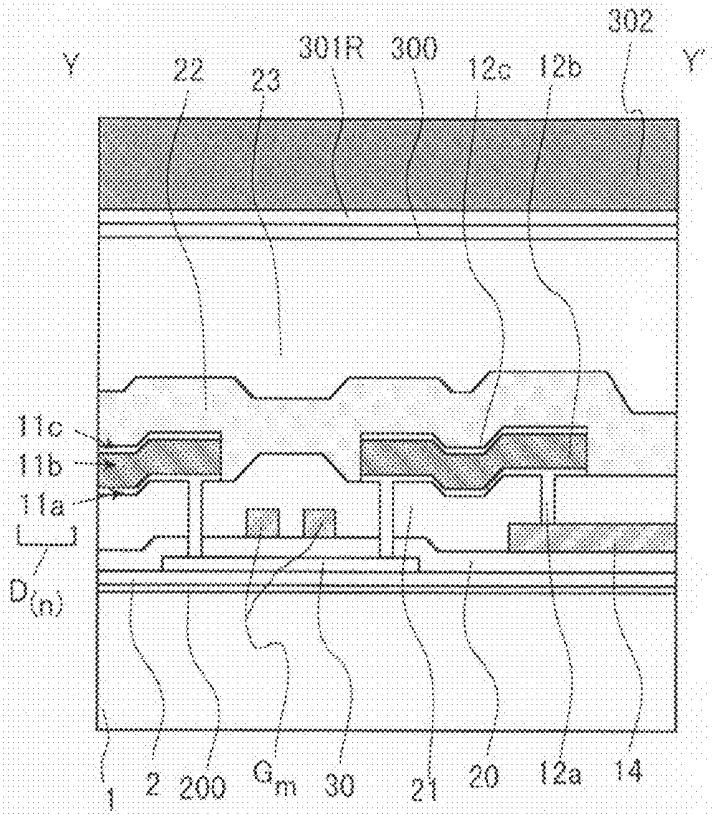

Y
22
23
301R
300
12c
12b
302
Y'
11c
11b
11a
D(n)
1
2
200
Gm
30
21
20
12a
14

FIG.9

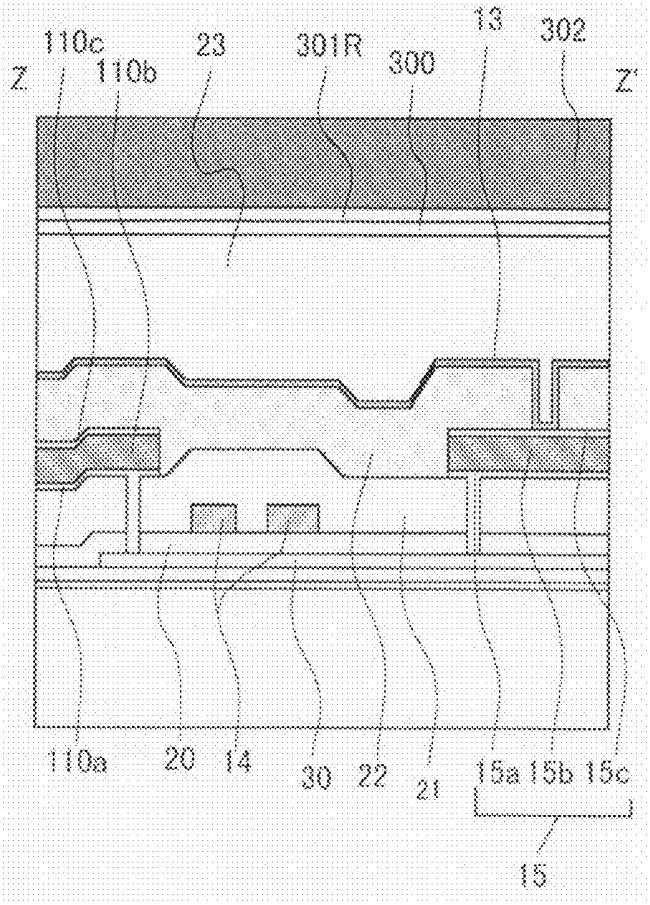

Z
110c
110b
23
301R
300
13
302
Z'
110a
20
14
30
22
21
15a
15b
15c
15

FIG.10

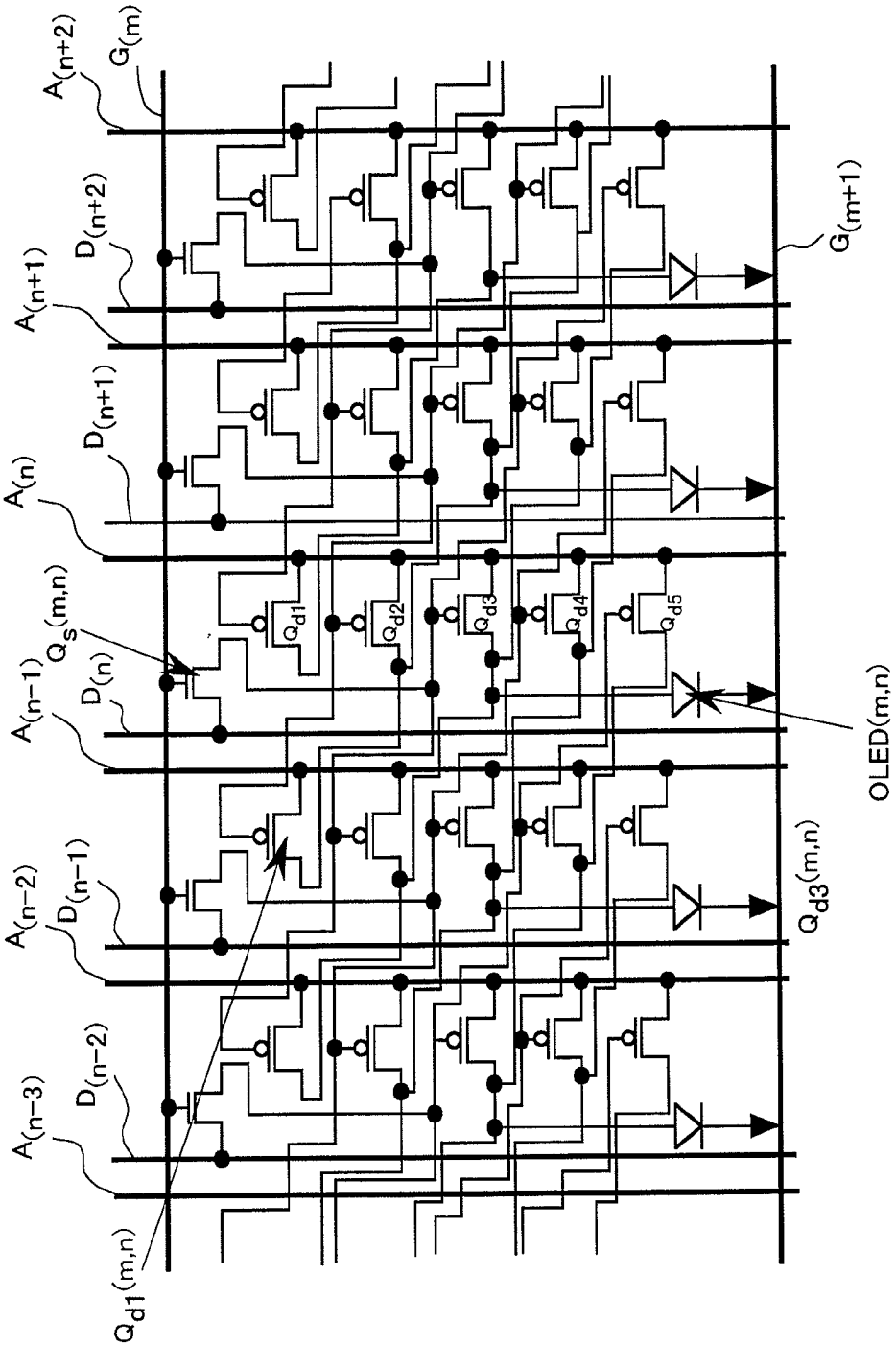

A(n+2)
G(m)
D(n+2)
A(n+1)
D(n+1)
A(n)
Qs(m,n)
D(n)
A(n-1)
D(n-1)
A(n-2)
D(n-2)
A(n-3)
Qd1(m,n)
Qd1
Qd2
Qd3
Qd4
Qd5
G(m+1)
OLED(m,n)
Qd3(m,n)

FIG.11

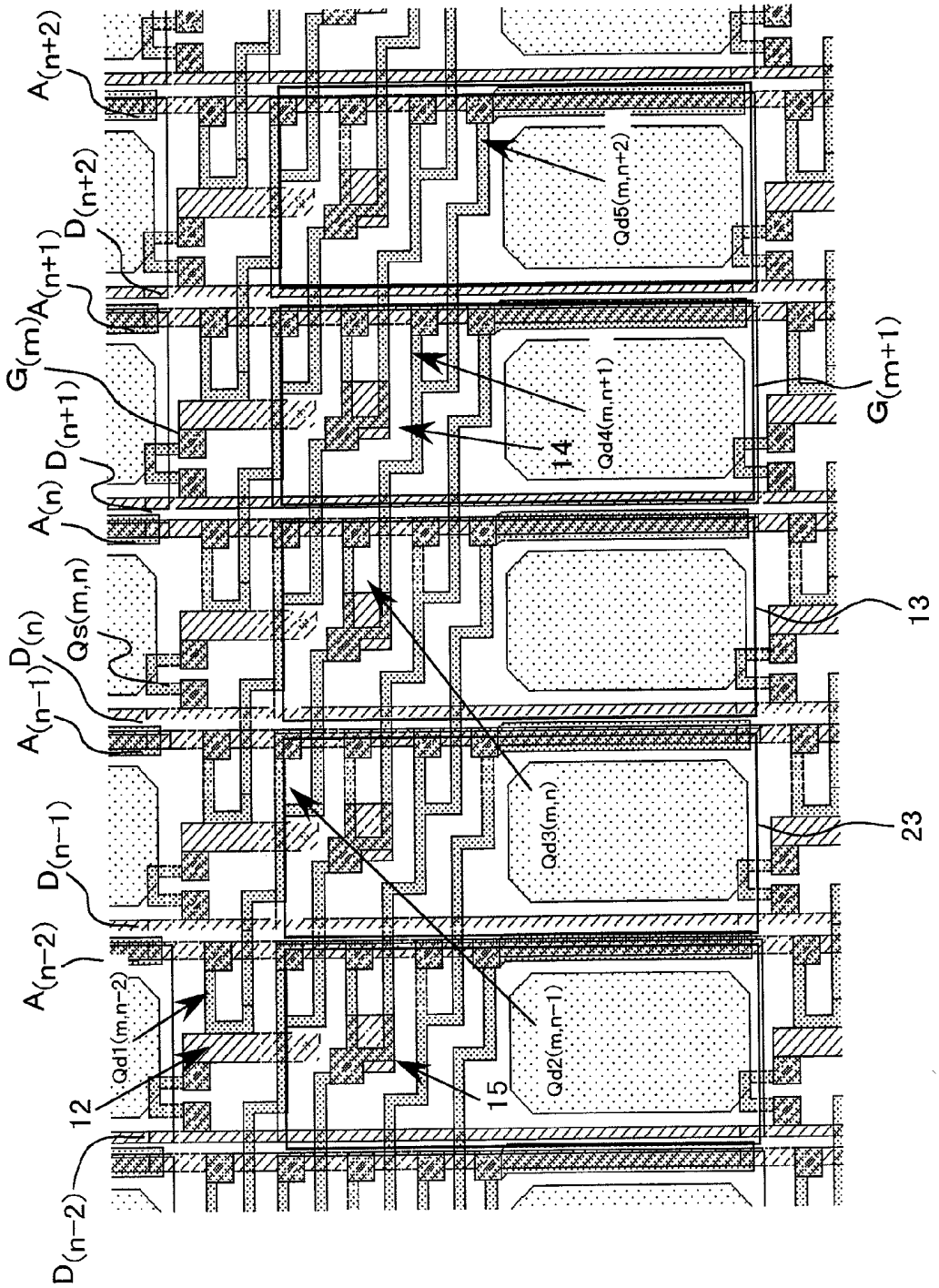

A(n+2)
D(n+2)
A(n+1)
G(m)
D(n+1)
A(n)
D(n)
Qs(m,n)
A(n-1)
D(n-1)
A(n-2)
D(n-2)
Qd1(m,n-2)
Qd2(m,n-1)
Qd3(m,n)
Qd4(m,n+1)
Qd5(m,n+2)
G(m+1)
12
13
14
15
23

FIG.12

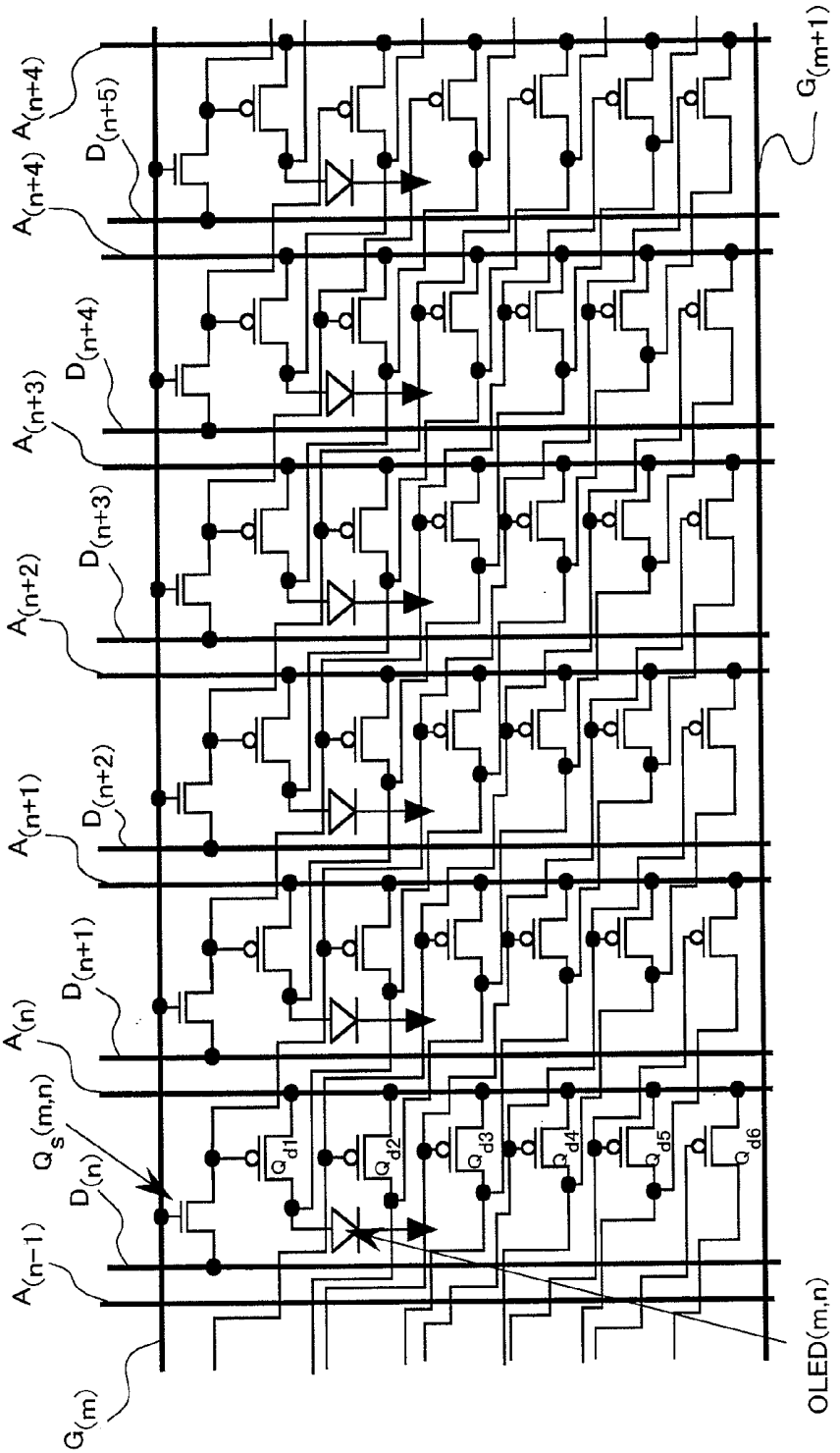

A(n-1)
A(n)
A(n+1)
A(n+2)
A(n+3)
A(n+4)
A(n+4)
D(n)
D(n+1)
D(n+2)
D(n+3)
D(n+4)
D(n+5)
Qs(m,n)
Qd1
Qd2
Qd3
Qd4
Qd5
Qd6
G(m)
G(m+1)
OLED(m,n)

FIG.13

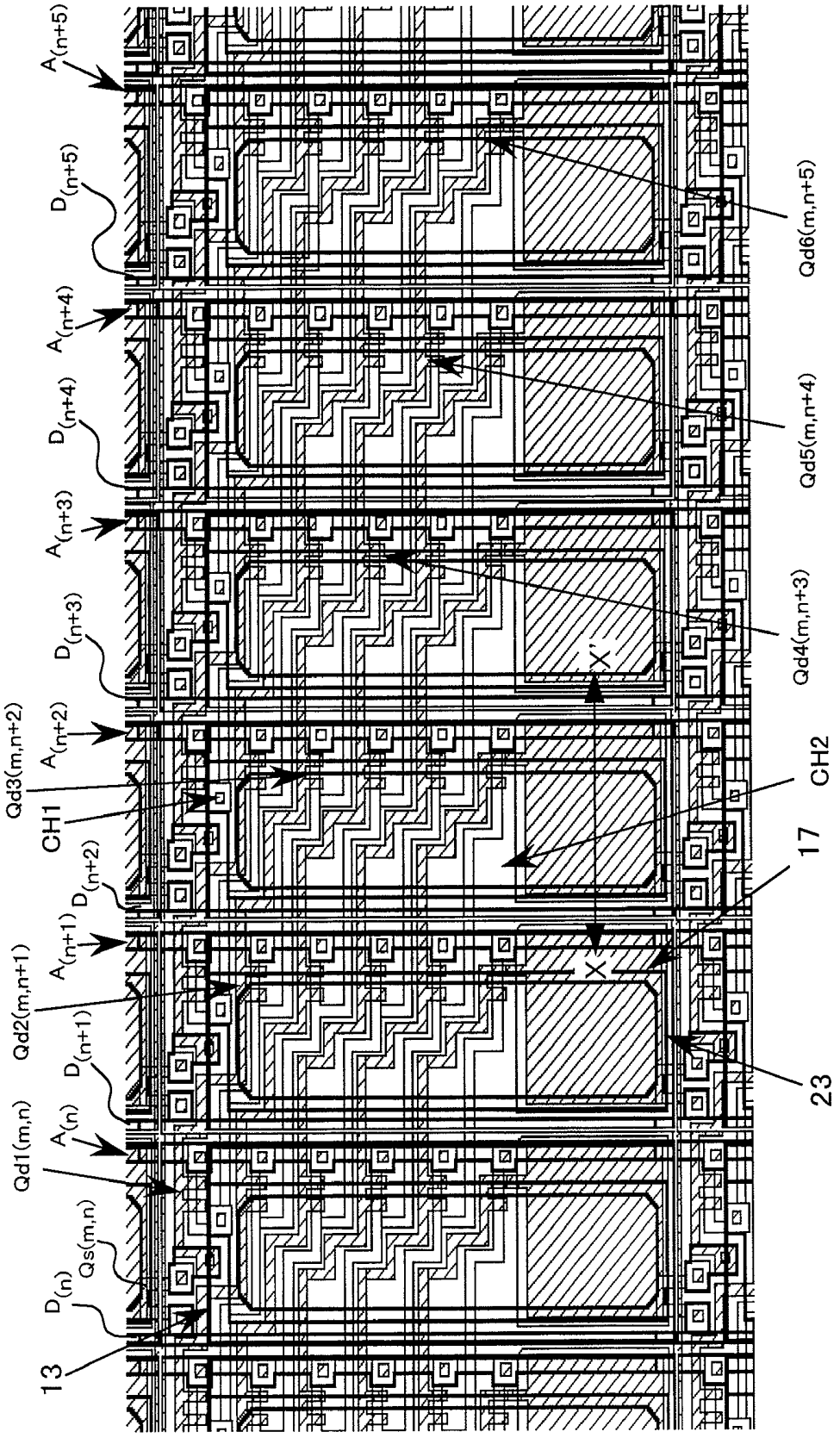

A(n+5)
D(n+5)
A(n+4)
D(n+4)
A(n+3)
D(n+3)
A(n+2)
D(n+2)
A(n+1)
D(n+1)
A(n)
D(n)
Qd6(m,n+5)
Qd5(m,n+4)
Qd4(m,n+3)
Qd3(m,n+2)
Qd2(m,n+1)
Qd1(m,n)
Qs(m,n)
CH1
CH2
X
X'
13
17
23

FIG.14

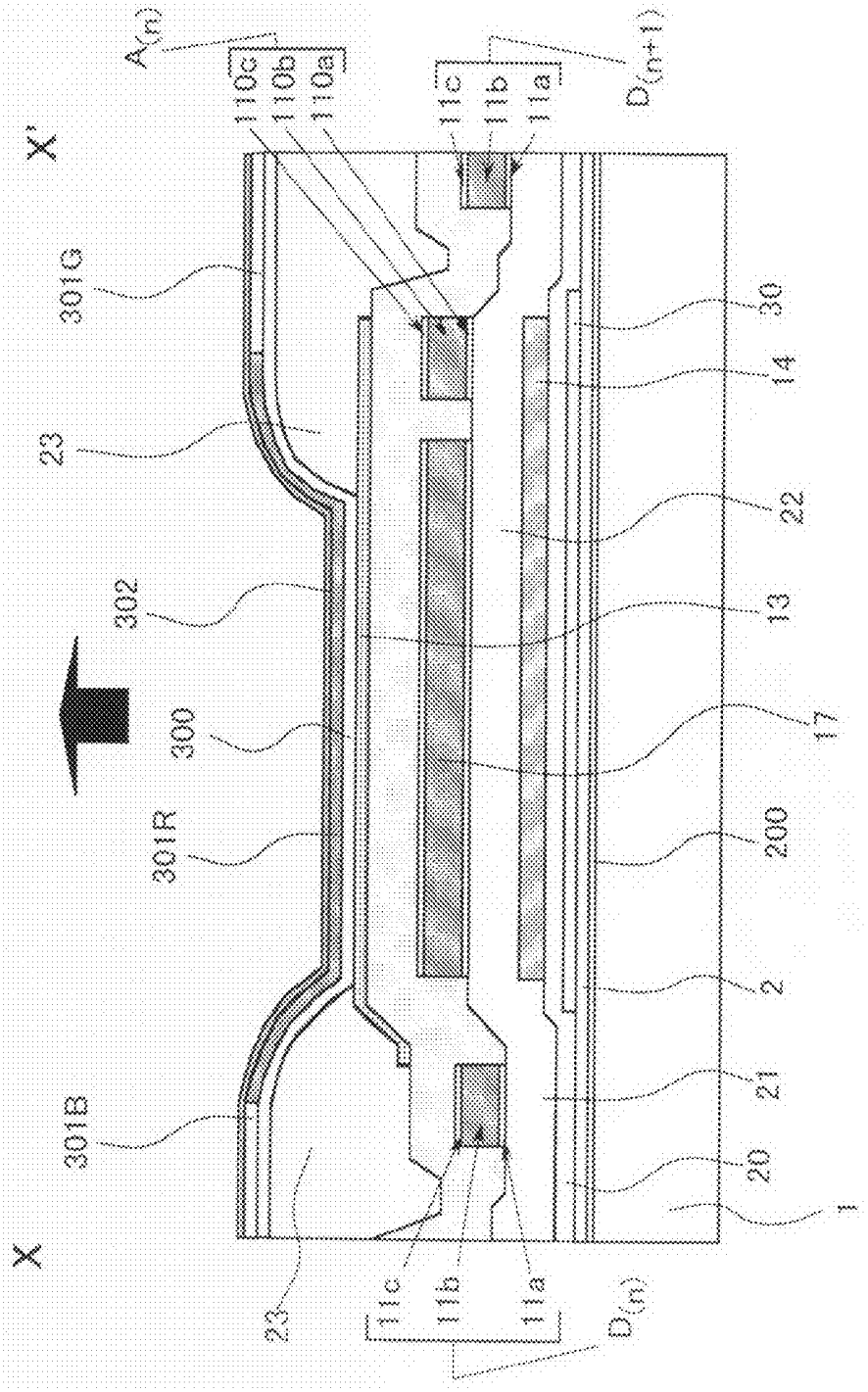

X'
X
$A_{(n)}$
110c
110b
110a
11c
11b
11a
$D_{(n+1)}$
301G
23
302
300
301R
301B
30
14
22
13
17
200
2
21
20
1
23
11c
11b
11a
$D_{(n)}$

FIG.15

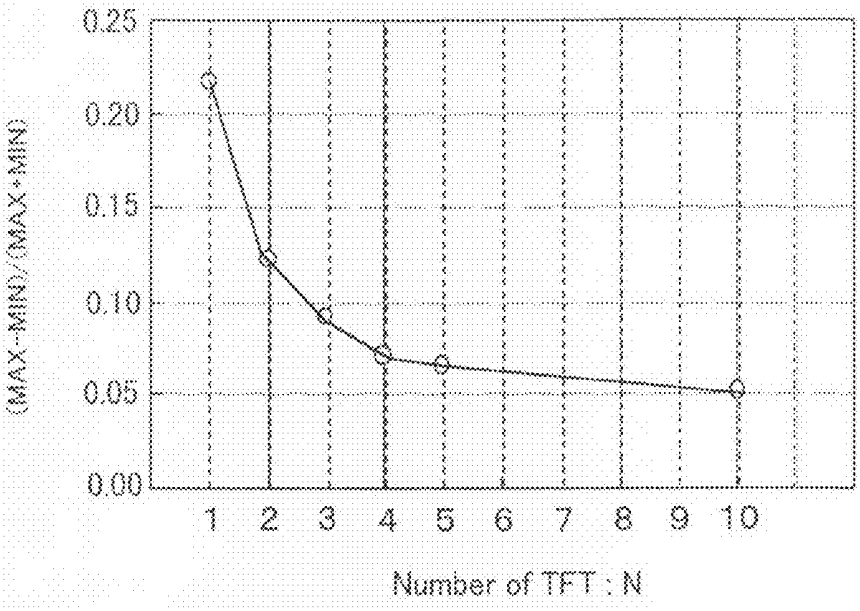
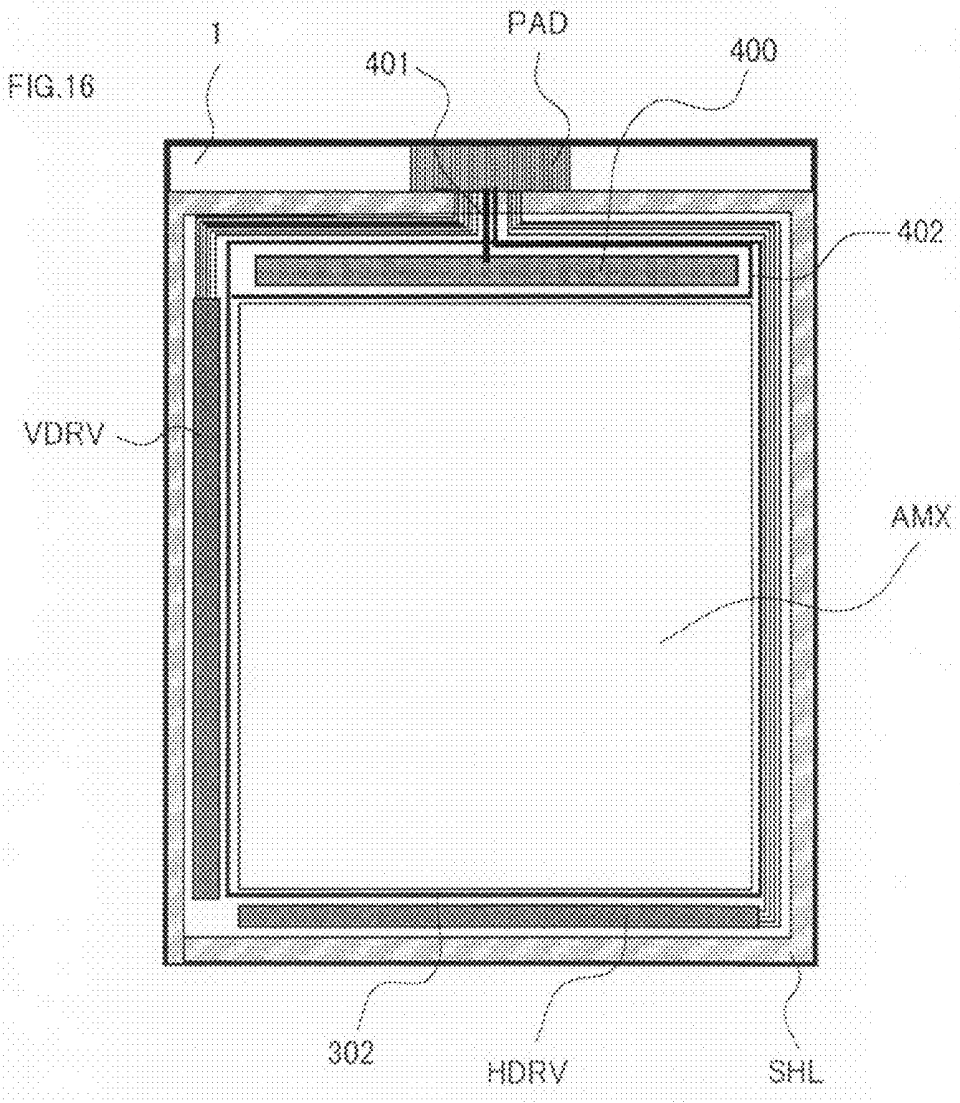

0.25
0.20
0.15
0.10
0.05
0.00
(MAX-MIN)/(MAX+MIN)
1 2 3 4 5 6 7 8 9 10
Number of TFT : N

FIG.16


1
PAD
401
400
402
VDRV
AMX
302
HDRV
SHL

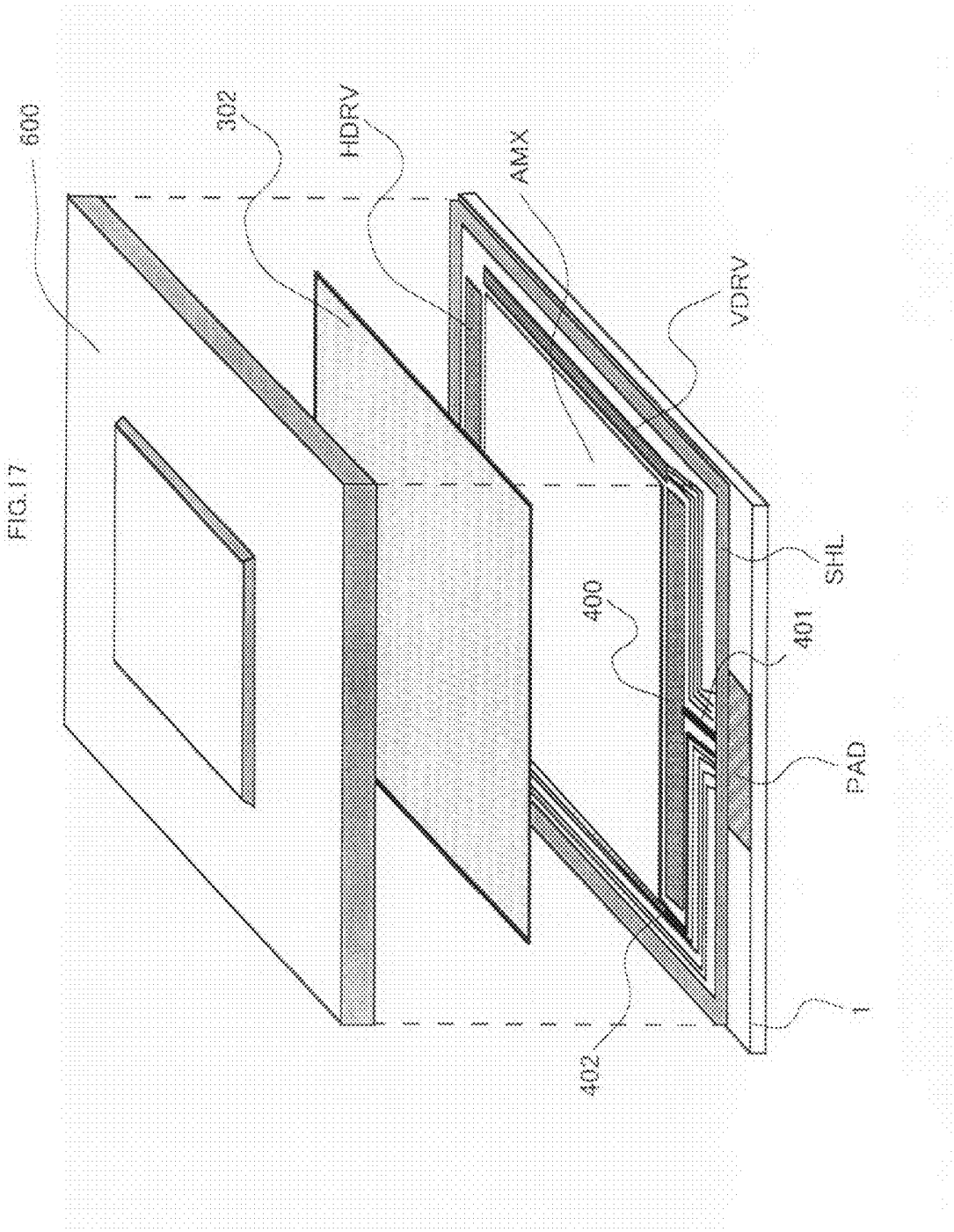


FIG.17

FIG.18

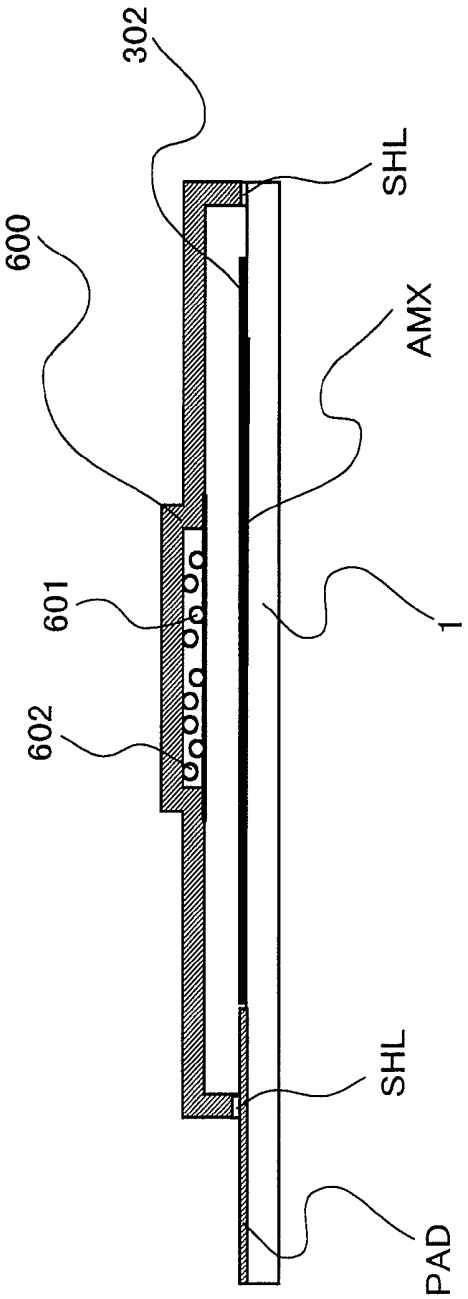
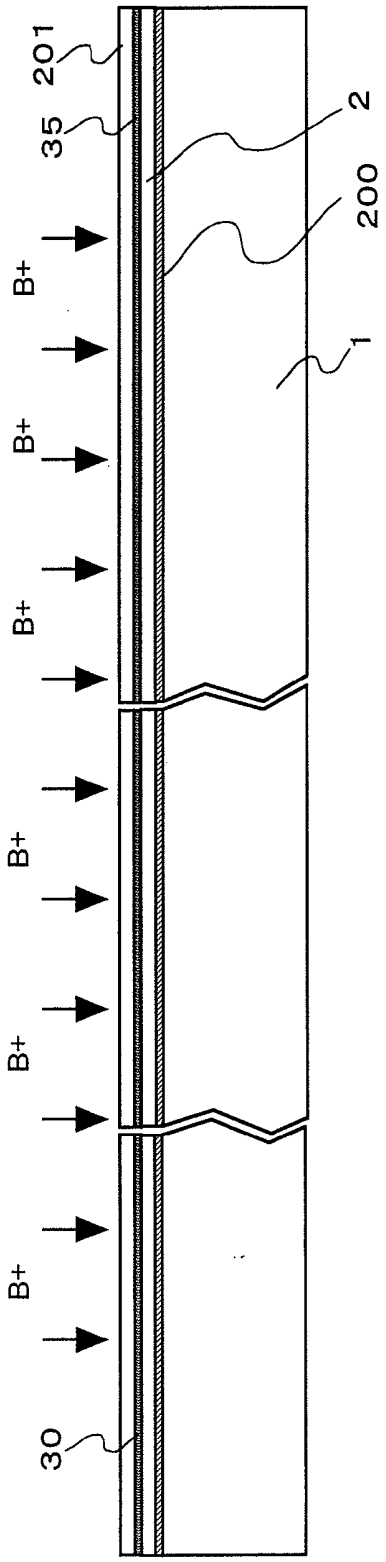


FIG.19



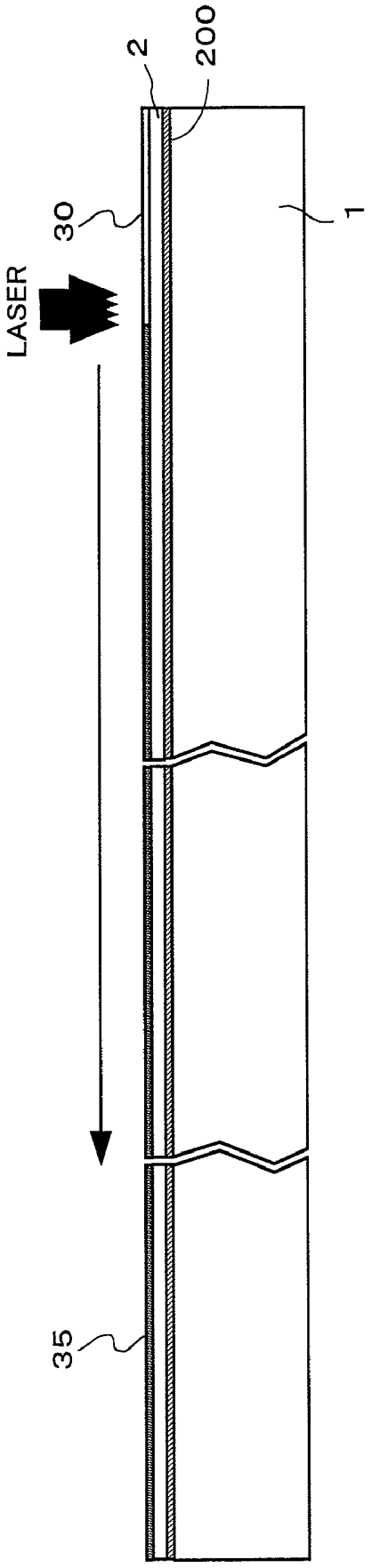


FIG.20

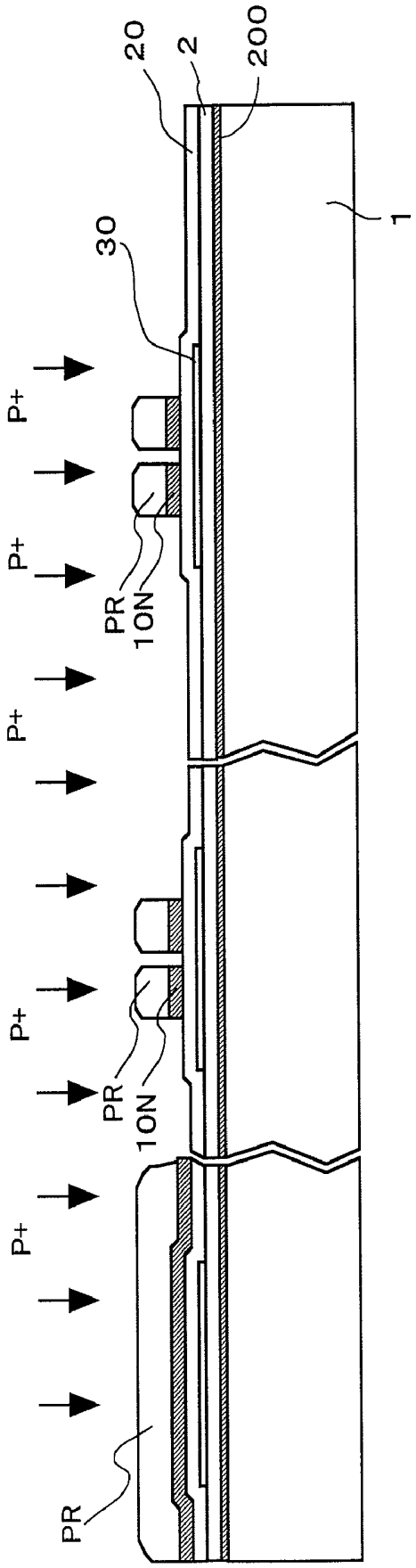


FIG.21

FIG.22

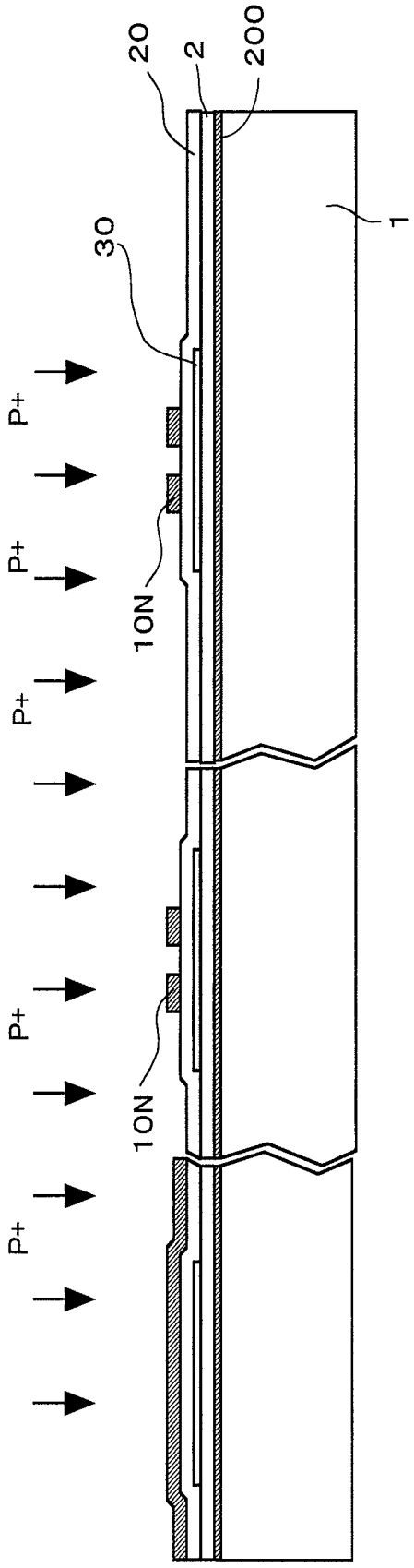
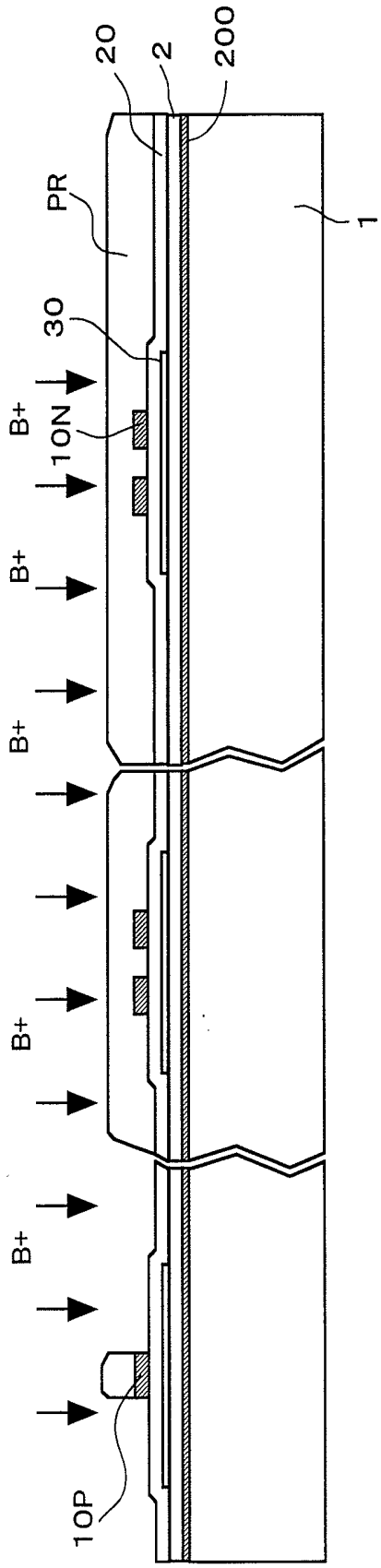


FIG.23



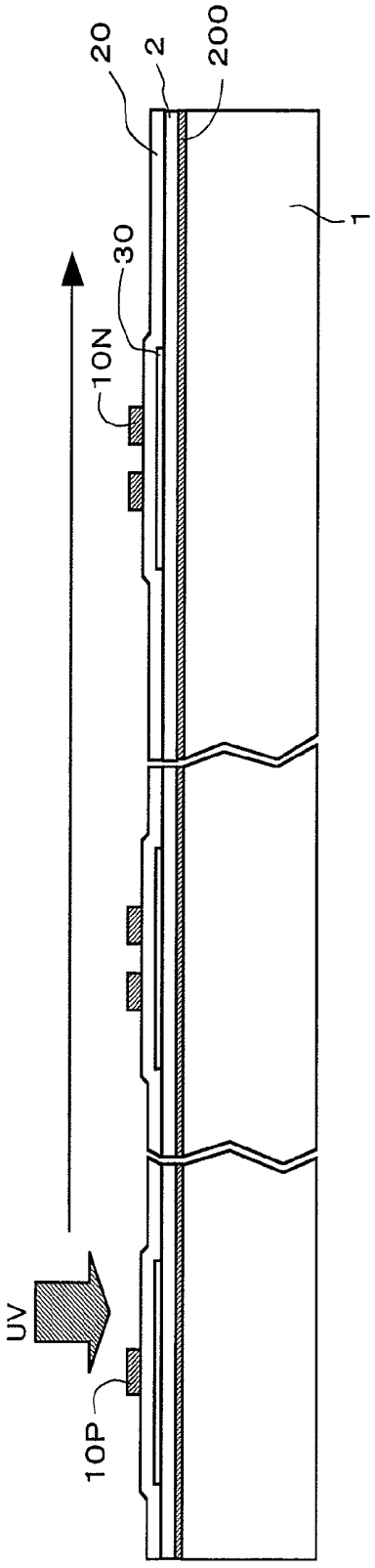


FIG.24

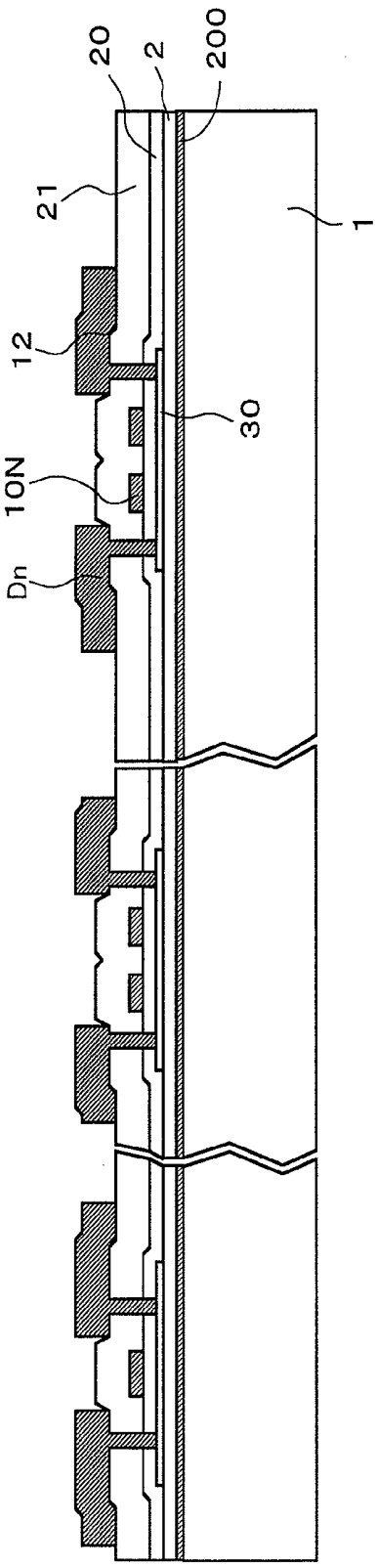


FIG.25

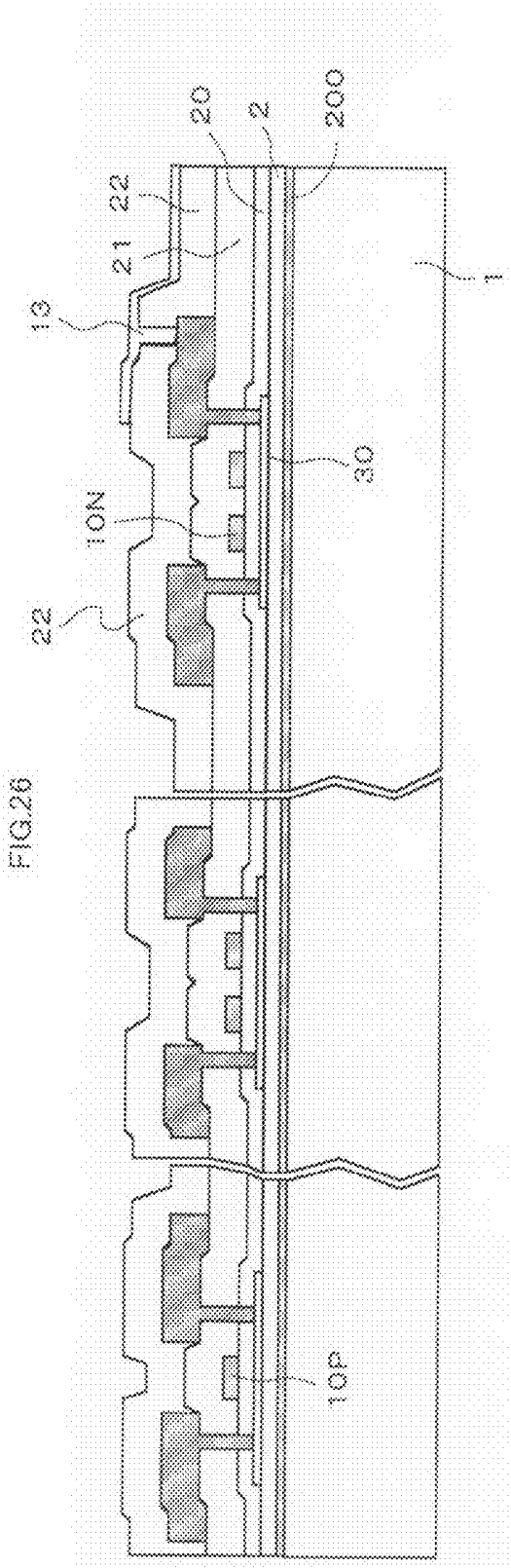


FIG.26

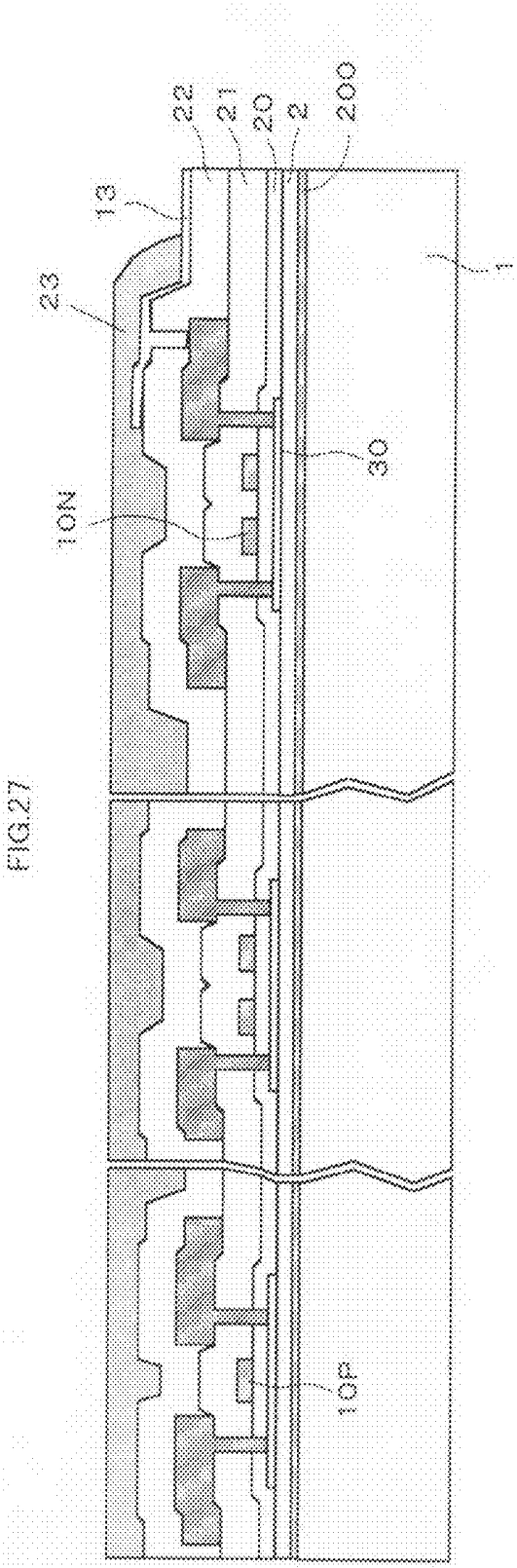


FIG.27

DISPLAY DEVICE INCLUDING AN ORGANIC EL DEVICE

CROSS REFERENCE TO RELATED APPLICATION

[0001] This is a continuation of U.S. application Ser. No. 11/634,089, filed Dec. 6, 2006, which, in turn, is a divisional of U.S. application Ser. No. 10/304,700, filed Nov. 27, 2002 (now U.S. Pat. No. 7,157,847). This application relates to and claims priority from Japanese Patent Application No. 2001-363915, filed on Nov. 29, 2001. The entirety of the contents and subject matter of all of the above is incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a display device and, more particularly, to a structure of an active matrix type organic electroluminescent display.

[0004] 2. Description of the Related Art

[0005] Active matrix driven organic electroluminescent displays (referred below to as AMOLED) is expected as flat panel displays of the next generation succeeding conventional liquid crystal displays.

[0006] Conventionally, a two-transistor structured circuit, as disclosed in JP-A-2000-163014 (first prior technique), comprising a drive thin-film transistor (referred below to as EL drive TFT) for feeding current to organic electroluminescent elements (referred below simply to as EL element), a holding capacitor connected to a gate electrode of the EL drive TFT for holding a picture signal voltage, and a switch thin-film transistor (referred below to as switch TFT) for feeding a picture signal voltage to the holding capacitor, has been known as a fundamental pixel circuit for a pixel drive circuit of AMOLED.

[0007] The two-transistor structured fundamental pixel circuit causes a significant problem that nonuniformity in a picture is caused by dispersion every pixel in a threshold voltage (Vth) and mobility (μ) of the EL drive TFT due to dispersion every location in the crystallizing property of a semiconductor thin film (for which a polycrystal silicon film is ordinarily used) constituting the EL drive TFT.

[0008] Since dispersion in threshold voltage and mobility results in dispersion in a drive current value of the EL element, emission intensity disperses to cause minute unevenness to be seen in representation.

Such unevenness in representation becomes particularly problematic when a drive current value is small to represent half tone.

[0009] Several measures have been devised in order to suppress that nonuniformity in representation, which is caused by such dispersion in the characteristics of an EL drive TFT.

[0010] For example, JP-A-11-219133 discloses a method, in which dispersion in a drive current value is suppressed by making channel length and channel width of an EL drive TFT fairly greater than an average crystal particle size of polycrystal silicon constituting the EL drive TFT (referred below to as second prior technique).

[0011] Also, JP-A-2000-3305027 discloses a drive method by a so-called pulse-width modulation, in which an EL drive TFT is driven as a binary switch for effecting a complete OFF state or a complete ON state and tone of a picture is represented by changing a duration of emission (referred below to as third prior technique).

[0012] Also, JP-A-11-73158 discloses an area tone system, in which a plurality of EL elements having different luminescent areas are provided in a unit pixel, and an EL drive TFT is connected to each of the plurality of EL elements and driven as a binary switch for effecting a complete OFF state or a complete ON state, whereby tone is represented by changing luminescent areas (referred below to as fourth prior technique).

[0013] Also, U.S. Pat. No. 6,229,506B1 discloses a method, in which four TFTs are provided in a pixel to constitute a circuit for cancelling dispersion in a threshold voltage of an EL drive TFT whereby dispersion in drive current is decreased (referred below to as fifth prior technique).

[0014] Also, JP-A-8-129359 discloses a method, in which a plurality of EL drive TFTs having different current drive capacities conformed to a plurality of tone currents are connected in parallel to one EL element within each pixel and driven as binary switches for effecting a complete OFF state or a complete ON state, whereby tone representation is controlled by tone currents supplied from the plurality of EL drive TFTs (referred below to as sixth prior technique).

[0015] Also, JP-A-2000-221903 discloses a method, in which two EL drive TFTs are provided in a pixel to decrease dispersion in threshold voltages in the EL drive TFTs, thereby reducing dispersion in drive current (referred below to as seventh prior technique).

[0016] However, the prior techniques described above involve the following problems.

[0017] The second prior technique is directed to averaging dispersion every location in the crystallizing property of the polycrystal silicon by increasing TFT size.

However, even when TFT size is increased, it cannot be made greater than pixel pitch.

[0018] Accordingly, since a size of an EL drive TFT for driving an EL element, which constitutes each pixel, is limited within an area of a pixel, and the crystallizing property of a polycrystal silicon film disperses every location, it is not possible to compensate for dispersion between the characteristics of an EL drive TFT in a particular pixel and the characteristics of an EL drive TFT in a pixel adjacent the particular pixel.

[0019] It is to be noted that what can be averaged by increasing a TFT size is only dispersion in crystals sized within the TFT size.

Accordingly, it is difficult in the second prior technique to obtain a fairly uniform property of representation.

[0020] For the effect of averaging picture representation with the third prior technique, the pulse-width modulation driving is one of valid methods as an AMOLED driving method as having already been proved.

[0021] However, known as an essential problem in this driving method is bleeding in a picture generated when animation called pseudo-profile is represented because tone representation is made by luminescence pulse, which is developed on time base.

[0022] Also, because of a need for processing a short signal pulse conformed to digital tone, there is caused a problem that the drive circuit is increased in operation frequency and power consumption.

[0023] Also, there is also caused a problem that a vertical scanning circuit, which may ordinarily be a simple circuit, becomes complex and a circuit area is increased.

[0024] The fourth prior technique is much effective in uniformizing picture representation, but multitone is difficult since it is necessary to form in a unit pixel EL elements having areas conformed to digital tone and to form EL drive TFTs corresponding to the respective EL elements.

[0025] Also, it has been known that EL elements are ordinarily decreased in luminescent areas together with operation duration.

In the case of using EL elements having different luminescent areas, deterioration is caused with time beginning with an EL element, which has a small area corresponding to a low-tone bit, thus causing also a problem that normal tone becomes difficult with time.

[0026] With the fifth prior technique, the provision of a circuit for canceling dispersion in threshold voltage of an EL drive TFT necessitates a wiring, which is not necessary in a conventional two-transistor configuration, so that a decrease in numerical aperture and yield in manufacture causes a problem.

[0027] Also, what can be cancelled is only dispersion in threshold voltage, and dispersion in mobility remains intact. Therefore, there is caused a problem that no fairly uniformizing effect is obtained on drive current.

[0028] With the sixth prior technique, a plurality of EL drive TFTs having current drive capacities conformed to digital tone are connected in parallel.

However, it is apparent that normal tone representation is made difficult when the plurality of EL drive TFTS disperse in characteristics.

[0029] Also, since the plurality of EL drive TFTs are formed in a single pixel in this method, the technique is in no way effective in decreasing dispersion in representation among a plurality of pixels.

[0030] With the seventh prior technique, dispersion in drive current can be decreased in the case where one of two EL drive TFTs connected in parallel is varied in characteristics, but dispersion in drive current cannot be decreased in the case where both the two EL drive TFTs are varied in characteristics, and besides the two EL drive TFTs are formed in a single pixel, so that the technique is in no way effective in decreasing dispersion in representation among a plurality of pixels.

SUMMARY OF THE INVENTION

[0031] The invention has been thought of in order to solve the problems of the above prior art, and has its object to provide a technique for display devices, in which dispersion in representation among a plurality of pixels, attributable to dispersion in characteristics of drive thin-film transistors is decreased and uniform representation free of unevenness can be obtained.

[0032] Also, another object of the invention is to provide a technique capable of decreasing voltage drop and power consumption caused by resistance of taken-out wirings of cathode electrodes in a display device.

[0033] The above and other objects and novel features of the invention will be made apparent from the descriptions in the specification of this application and the accompanying drawings.

[0034] An outline of a typical one of the inventions disclosed in this application will be simply described below.

[0035] That is, the invention has a feature in that a plurality of EL drive TFTs are connected in parallel to current drive type luminescent elements arranged in respective pixel regions, current is supplied to the current drive type luminescent elements from a plurality of current supply sources, and the plurality of EL drive TFTs are arranged in a plurality of pixel regions at intervals corresponding substantially to pitch of pixel.

[0036] The plurality of EL drive TFTs are connected in parallel whereby it is possible to average dispersion in drive current, attributable to dispersion in threshold voltage and mobility among the plurality of EL drive TFTS.

However, only making EL drive TFTs in plural and in parallel does not assure averaging dispersion in drive current for an EL drive TFT corresponding to a particular pixel and, for example, pixels adjacent to the particular pixel.

[0037] Nonuniformity in representation is caused by dispersion in drive current for EL drive TFTs in a plurality of pixels, which dispersion is attributable to dispersion in the crystallizing property of a semiconductor film constituting TFTs and spatial dispersion in filmy nature of an insulating film.

[0038] Since EL drive TFTs are arranged regularly at the same intervals as array pitch of pixels, it may be thought that dispersion in drive current is attributable to dispersion in the crystallizing property of a semiconductor film and spatial dispersion in filmy nature of an insulating film on a scale of array pitch of pixels.

[0039] In order to average such dispersion, it is effective to spatially disperse and arrange the plurality of EL drive TFTs at array pitch of pixels.

[0040] Accordingly, a plurality of EL drive TFTs are connected in parallel to current drive type luminescent elements arranged in respective pixel regions, current is supplied to the current drive type luminescent elements from a plurality of current supply sources, and the plurality of EL drive TFTs are arranged in a plurality of pixel regions at intervals corresponding substantially to pitch of pixel, whereby dispersion in drive current supplied to the current drive type luminescent elements corresponding to respective pixels can be decreased and representation can be averaged.

[0041] The more the averaging effect by means of the plurality of EL drive TFTs distributed and arranged spatially, the more the number of TFTs connected in parallel.

[0042] It is theoretically predicted that the magnitude of dispersion in drive current decreases inversely proportional to $\sqrt{N}$ with an increase in N when the number in parallel is N. Since pixels are limited in size, N=2 to 12 is a practical value according to the rule of fine processing thin-film transistors (TFT) in the present circumstances.

[0043] Also, when the number of TFTs in a pixel is increased, it is difficult to ensure an area for EL elements, which contribute to emission of light.

[0044] According to the invention, numerical aperture is enhanced by providing a reflective layer in a manner to cover at least a part of EL drive TFTs and forming current drive type luminescent elements on the reflective layer.

[0045] Also, since current from the luminescent elements in all pixels flows through taken-out wirings of cathode electrodes of current drive type luminescent elements arranged in respective pixel regions, it is important to decrease resistance of the taken-out wirings.

[0046] According to the invention, voltage drop and power consumption caused by resistance of taken-out wirings are

minimized by shortening lengths of the taken-out wirings, which are connected electrically to cathode electrodes of a plurality of current drive type luminescent elements, extending from an external connection terminal to a contact area.

[0047] Concrete examples will be shown in the following embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0048] FIG. **1** is a circuit diagram showing equivalent networks for pixels in a display device according to a first embodiment of the invention;

[0049] FIG. **2** is a plan view showing a pixel arrangement in the display device according to the first embodiment of the invention;

[0050] FIG. **3** is a circuit diagram showing an entire display unit including equivalent networks and a driving circuit in a matrix display section of the display device according to the first embodiment of the invention;

[0051] FIG. **4** is a circuit diagram showing equivalent networks for pixels in a display device according to a second embodiment of the invention;

[0052] FIG. **5** is a plan view showing a pixel arrangement in the display device according to the second embodiment of the invention;

[0053] FIG. **6** is a circuit diagram showing an entire display unit including equivalent networks and a driving circuit in a matrix display section of the display device according to the second embodiment of the invention;

[0054] FIG. **7** is a cross sectional view showing a cross-sectional structure cut along the line X-X' shown in FIG. **5**;

[0055] FIG. **8** is a cross sectional view showing a cross-sectional structure cut along the cut line Y-Y' shown in FIG. **5**;

[0056] FIG. **9** is a cross sectional view showing a cross-sectional structure cut along the cut line Z-Z' shown in FIG. **5**;

[0057] FIG. **10** is a circuit diagram showing equivalent networks for pixels in a display device according to a third embodiment of the invention;

[0058] FIG. **11** is a plan view showing a pixel arrangement in the display device according to the third embodiment of the invention;

[0059] FIG. **12** is a circuit diagram showing equivalent networks for pixels in a display device according to a fourth embodiment of the invention;

[0060] FIG. **13** is a plan view showing a pixel arrangement in the display device according to the fourth embodiment of the invention;

[0061] FIG. **14** is a cross sectional view showing a cross-sectional structure cut along the line X-X' shown in FIG. **13**;

[0062] FIG. **15** is a graph indicating the relationship between the number N of thin-film transistors for driving parallel organic electroluminescence elements and dispersion in luminance among pixels;

[0063] FIG. **16** is a plan view showing an entire configuration of display devices according to the respective embodiments of the invention;

[0064] FIG. **17** is an exploded, perspective view showing an entire configuration of display devices according to the respective embodiments of the invention;

[0065] FIG. **18** is a cross sectional view showing an essential part of a cross-sectional structure of display devices according to the respective embodiments of the invention;

[0066] FIG. **19** is a view illustrating the manufacturing process of the display device according to the second embodiment of the invention;

[0067] FIG. **20** is a view illustrating the manufacturing process of the display device according to the second embodiment of the invention;

[0068] FIG. **21** is a view illustrating the manufacturing process of the display device according to the second embodiment of the invention;

[0069] FIG. **22** is a view illustrating the manufacturing process of the display device according to the second embodiment of the invention;

[0070] FIG. **23** is a view illustrating the manufacturing process of the display device according to the second embodiment of the invention;

[0071] FIG. **24** is a view illustrating the manufacturing process of the display device according to the second embodiment of the invention;

[0072] FIG. **25** is a view illustrating the manufacturing process of the display device according to the second embodiment of the invention;

[0073] FIG. **26** is a view illustrating the manufacturing process of the display device according to the second embodiment of the invention; and

[0074] FIG. **27** is a view illustrating the manufacturing process of the display device according to the second embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0075] Embodiments according to the invention will be described in detail with reference to the drawings.

[0076] In addition, the same numerals and letters denote elements having the same functions in all the drawings, which illustrate embodiments, and repeated explanations therefor are omitted.

First Embodiment

[0077] FIG. **1** is a circuit diagram showing equivalent networks for pixels in a display device according to a first embodiment of the invention, and FIG. **2** is a plan view showing a pixel arrangement in the display device according to the first embodiment of the invention.

[0078] In a self-luminescence display device according to the invention, organic electroluminescent elements (referred simply below to as EL elements) of respective pixels are driven by three drive thin-film transistors (referred below to as EL drive TFT) provided on different pixel regions.

[0079] In the first embodiment, respective EL drive TFTs are arranged in an associated pixel, the next pixel on the right side and the further next pixel but one on the right side.

[0080] In FIG. **1**, there are shown three pixel regions surrounded by scanning signal wiring electrodes (Gm, G(m+1)), picture signal wiring electrodes (Dn to D(n+1)), and anode current feeding wiring electrodes (A(n−1) to A(n+2)), which constitute a part of a TFT matrix.

[0081] A pixel in a row m and a column n is defined by a region surrounded by scanning signal wiring electrodes (Gm, G(m+1)), a picture signal wiring electrodes Dn, and an anode current feeding wiring electrode An.

[0082] Formed in respective pixels are switch thin-film transistors (referred below to as switch TFT) (Qs(m, n)), three EL drive TFTs (Qd**1**(*m, n*), Qd**2**(*m, n*), Qd**3**(*m, n*)), and a charge-storage capacitance Cst(m, n).

[0083] An anode electrode of an EL element OLED(m, n) is connected to a drain electrode of the EL drive TFT (Qd**1**(*m, n*)) via an EL connection wiring electrode **15**.

[0084] The EL element OLED(m, n) belonging to a pixel in row m and column n is connected not only to the EL drive TFT (Qd**1**(*m, n*)) in the pixel but also in parallel to the EL drive TFT (Qd**2**(*m, n*+1)) formed in an adjacent pixel in row m and column (n+1) and the EL drive TFT (Qd**3**(*m, n*+2)) formed in an pixel in row m and column (n+2) such that current is fed from three anode current feeding wiring electrodes (An, A(n+1), A(n+2)).

[0085] All gate wiring electrodes **14** of the three parallel-connected EL drive TFTs are connected to a drain electrode of a switch TFT (Qs(m,n)) of a pixel in row m and column n via an EL connection wiring electrode **12**.

[0086] Also, a charge-storage capacitance Cst (m, n+2) is formed between gate electrode nodes of the three EL drive TFTs and the anode current feeding wiring electrode A(n+2) to be able to keep voltage of the gate wiring electrodes **14** for a predetermined period of time.

[0087] In the embodiment, scanning signal wiring electrodes G are sequentially scanned, and a switch TFH (Qs), to which a scanning signal wiring electrode G made at H level is connected, is made ON.

Thereby, a picture signal voltage is fed via the switch TFH (Qs) to a charge-storage capacitance Cst from the picture signal wiring electrodes Dn to be held on the charge-storage capacitance Cst.

[0088] Based on the picture signal voltage held on the charge-storage capacitance Cst, the respective EL drive TFTs (Qd**1**, Qd**2**, Qd**3**) feed to the EL elements OLED current corresponding to the picture signal voltage held on the charge-storage capacitance Cst during one frame.

[0089] Thereby, the EL elements OLED emit light to display a picture image.

[0090] In addition, with the embodiment, gate length, channel length, and channel width are set so that current fed to the respective EL drive TFTs (Qd**1**, Qd**2**, Qd**3**) becomes substantially equal to a current fed by a single EL drive TFT.

[0091] In the embodiment, the respective EL drive TFTs (Qd**1**(*m,n*), Qd**2**(*m,n*), Qd**3**(*m,n*)) are of a double gate structure to have a gate length of 10 μm, total channel length of 20 μm, and a channel width of 4 μm.

[0092] Supplying of current to the EL elements OLED(m, n) from the EL drive TFT (Qd**2**(*m, n*+1)) and the EL drive TFT (Qd**3**(*m, n*+2)) is made by extending p+type semiconductor layers, which constitute source electrodes and drain electrodes of the respective EL drive TFTS, as they are and using the same as wiring.

[0093] With such configuration, since formation of surplus contact through holes is made unnecessary, surface efficiency is enhanced with the result that numerical aperture is improved.

[0094] Take again notice of a pixel in row m and column n, the EL drive TFT (Qd**2**(*m,n*)) among the three EL drive TFTs (Qd**1**(*m,n*), Qd**2**(*m,n*), Qd**3**(*m,n*)) is provided to drive an EL element OLED(m, n−1) of a pixel in row m and column (n−1), and the EL drive TFT (Qd**3**(*m,n*)) is provided to drive an EL element OLED(m, n−2) of a pixel in row m and column (n−2).

[0095] Also, the charge-storage capacitance Cst(m, n) is provided to hold an electric potential of a gate electrode node of the EL drive TFT (Qd**3**(*m,n*)).

[0096] The EL elements are formed on ITO electrodes (anode electrodes of the EL elements) **13**, which are connected to the EL connection wiring electrodes **15** via contact through holes, through openings formed on organic insulating films **23**.

[0097] FIG. **3** is a circuit diagram showing an entire display unit including equivalent networks and a driving circuit in a matrix display section of the display device according to the first embodiment.

[0098] As shown in FIG. **3**, the matrix display section is composed of 600 scanning signal wiring electrodes G**1** to G**600**, **2400** picture signal wiring electrodes D**1**R to D**800**R, D**1**G to D**800**G, and D**1**B to D**800**B, **2400** anode current feeding wiring electrodes A**1**R to A**800**R, A**1**G to A**800**G, and A**1**B to A**800**B, and pixels provided in regions where these electrodes intersect.

[0099] The matrix display section is driven by a vertical scanning circuit VDRV and a picture signal circuit HDRV, and the anode current feeding wiring electrodes arranged on the respective pixels are short-circuited outside the regions of pixels to be connected to an external electric power source.

[0100] In the embodiment, since the EL drive TFTs are arranged in an associated pixel, the next pixel on the right side and the further next pixel, two rows of dummy regions of pixels are provided outside a rightmost row of pixels.

[0101] Further, two anode current feeding wiring electrodes (A**02**, A**03**) are provided corresponding to the two rows of dummy regions of pixels outside the rightmost row of pixels.

[0102] Thus three anode current feeding wiring electrodes can also feed a specified current to the rightmost row of pixels via three EL drive TFTS.

[0103] Here, three pixels, in which three EL drive TFTs are arranged as shown in FIG. **3**, are ones arranged in the same direction as a laser scanning direction of laser used when EL drive TFTs are manufactured.

[0104] In this manner, EL drive TFTs are scattered to be arranged in a plurality of pixels, and connected in parallel to drive one EL element, whereby current for the EL drive TFTs is averaged and so dispersion in drive current between pixels can be reduced to improve uniformity in display.

[0105] Also, since three anode current feeding wiring electrodes feed current to one EL element via three EL drive TFTs at the same time, redundancy is provided for deficiency in display, which is caused by breaking of anode current feeding wiring electrodes and failure in opening of EL drive TFTs, thus enabling enhancing yield in manufacture.

Second Embodiment

[0106] FIG. **4** is a circuit diagram showing equivalent networks for pixels in a display device according to a second embodiment of the invention, and FIG. **5** is a plan view showing a pixel arrangement in the display device according to the second embodiment of the invention.

As described above, with the self-luminescence display device according to the invention, EL elements of respective pixels are driven by three EL drive TFTs provided on different pixel regions.

[0107] In the embodiment, respective EL drive TFTs are arranged in an associated pixel, and the next pixels on the right and left sides.

[0108] FIG. **4** shows three regions of pixels surrounded by scanning signal wiring electrodes (Gm, G(m+1)), picture signal wiring electrodes (D(n−1) to D(n+2)), anode current feeding wiring electrodes (A(n−2) to A(n+1)), which constitute a part of the matrix.

[0109] A pixel in row m and column n is defined by a region, which is surrounded by scanning signal wiring electrodes (Gm, G(m+1)), a picture signal wiring electrode Dn and an anode current feeding wiring electrode An, and there are formed in the pixel a switch TFT (Qs(m, n)), three EL drive TFTs (Qd**1**(*m,n*), Qd**2**(*m,n*), Qd**3**(*m,n*)), and a charge-storage capacitance Cst(m, n).

[0110] An anode electrode of an EL element OLED (m, n) is connected to a drain electrode of the EL drive TFT (Qd**2**(*m, n*)) via an EL connection wiring electrode **15**.

[0111] An EL element OLED(m, n) belonging to a pixel in row m and column n is connected not only to the EL drive TFT (Qd**2**(*m, n*)) in the pixel but also in parallel to an EL drive TFT (Qd**3**(*m, n*+1)) formed in an adjacent pixel in row m and column (n+1) and an EL drive TFT (Qd**1**(*m, n*−1)) formed in an pixel in row m and column (n−1) such that current is fed from three anode current feeding wiring electrodes (A(n−1), An, A(n+1)).

[0112] All gate wiring electrodes **14** of the three parallel-connected EL drive TFTs are connected to a drain electrode of a switch TFT (Qs(m,n)) of a pixel in row m and column n via an EL connection wiring electrode **12**.

[0113] Also, a charge-storage capacitance Cst (m, n+1) is formed between gate electrode nodes of the three EL drive TFTs and the anode current feeding wiring electrode A(n+1) to be able to keep voltage of the gate wiring electrodes **14** for a predetermined period of time.

[0114] With the embodiment, gate length, channel length, and channel width are set so that current fed to the respective EL drive TFTs (Qd**1**, Qd**2**, Qd**3**) becomes substantially equal to a current fed by a single EL drive TFT.

[0115] In the embodiment, the respective EL drive TFTs (Qd**1**(*m,n*), Qd**2**(*m,n*), Qd**3**(*m,n*)) are of a double gate structure to have a gate length of 10 μm, total channel length of 20 μm, and a channel width of 4 μm.

[0116] Supplying of current to the EL elements OLED(m, n) from the EL drive TFT (Qd**1**(*m, n*−1)) and the EL drive TFT (Qd**3**(*m, n*+1)) is made by extending p+type semiconductor layers, which constitute source electrodes and drain electrodes of the respective EL drive TFTS, as they are and using the same as wiring.

[0117] With such configuration, since formation of surplus contact through holes is made unnecessary, surface efficiency is enhanced with the result that numerical aperture is improved.

[0118] Taking again notice of a pixel in row m and column n, the EL drive TFT (Qd**1**(*m,n*)) among the three EL drive TFTs (Qd**1**(*m,n*), Qd**2**(*m,n*), Qd**3**(*m,n*)) is provided to drive an EL element OLED(m, n+1) of a pixel in row m and column (n+1), and the EL drive TFT (Qd**3**(*m,n*)) is provided to drive an EL element OLED(m, n−1) of a pixel in row m and column (n−1).

[0119] Also, the charge-storage capacitance Cst(m, n) is provided to hold an electric potential of a gate electrode node of the EL drive TFT (Qd**3**(*m,n*)).

[0120] The EL elements are formed on ITO electrodes (anode electrodes of the EL elements) **13**, which are connected to the EL connection wiring electrodes **15** via contact through holes, through openings formed on an organic insulating film **23**.

[0121] FIG. **6** is a circuit diagram of an entire display unit including equivalent networks and a driving circuit in a matrix display section of the display device according to the second embodiment.

[0122] As shown in FIG. **6**, the matrix display section is composed of 600 scanning signal wiring electrodes G**1** to G**600**, **2400** picture signal wiring electrodes D**1**R to D**800**R, D**1**G to D**800**G, and D**1**B to D**800**B, **2400** anode current feeding wiring electrodes A**1**R to A**800**R, A**1**G to A**800**G, and A**1**B to A**800**B, and pixels provided in regions where these electrodes intersect.

[0123] The matrix display section is driven by a vertical scanning circuit VDRV and a picture signal circuit HDRV, and the anode current feeding wiring electrodes arranged on the respective pixels are short-circuited outside the regions of pixels to be connected to an external electric power source.

[0124] In the embodiment, since the EL drive TFTs are arranged in an associated pixel, and the next pixels on the right and left sides, two rows of dummy regions of pixels are provided on both sides of leftmost and rightmost rows of pixels, respectively.

[0125] Further, two anode current feeding wiring electrodes (A**00**, A**01**) are provided corresponding to the dummy pixels formed on the leftmost and rightmost rows of pixels.

[0126] Thus three anode current feeding wiring electrodes can also feed a specified current to the leftmost and rightmost row of pixels via three EL drive TFTs.

[0127] In this manner, EL drive TFTs are scattered to be arranged in a plurality of pixels, and connected in parallel to drive one EL element, whereby current for the EL drive TFTs is averaged and so dispersion in drive current between pixels can be reduced to improve uniformity in display.

[0128] Also, since three anode current feeding wiring electrodes feed current to one EL element via three EL drive TFTs at the same time, redundancy is provided for deficiency in display, which is caused by breaking of anode current feeding wiring electrodes and failure in opening of EL drive TFTs, thus enabling enhancing yield in manufacture.

[0129] In the embodiment, the number of EL drive TFTs arranged in parallel is three, and the EL drive TFTs are arranged in an associated pixel, and the next pixels on the right and left sides.

[0130] In comparing with the embodiment described above, lengths of the current feeding wiring electrodes constituted by p+type semiconductor layers from the EL drive TFT (Qd**1**(*m,n*−1)) and the EL drive TFT (Qd**3**(*m,n*+1)) to the EL element OLED(m, n) can be made substantially the same.

[0131] Thereby, sums of wiring resistances of the EL drive TFT and the p+type semiconductor layers from the anode current feeding wiring electrode A(n+1) and the anode current feeding wiring electrode A(n+1) to the EL element OLED(m, n) can be made substantially the same.

[0132] Since the wiring resistance of the p+type semiconductor layers is ordinarily set to be lower than the ON resistance of the EL drive TFT, unbalance in the wiring resistance of the p+type semiconductor layers causes no significant problem but an error is caused when wiring length is increased.

[0133] An error due to unbalance in the wiring resistance of the p+type semiconductor layers can be minimized by arranging EL drive TFTs in the next pixels on both sides as in the embodiment.

[0134] FIG. **7** is a cross sectional view showing a cross-sectional structure cut along the line X-X' shown in FIG. **5**.

[0135] As shown in FIG. **7**, a buffer Si_3N_4 film **200** having a thickness of 50 nm and a buffer SiO_2 film **2** having a

thickness of 100 nm are formed on a non-alkali glass substrate **1** having a thickness of 0.5 mm and a strain temperature of about 670° c.

[0136] These buffer insulating films (**200**, **2**) serve to prevent dispersion of impurities, such as Na or the like, from the glass substrate **1**.

[0137] Formed on the buffer SiO_2 film **2** is a polycrystal Si (referred below to as poly-Si) film **30** having a thickness of 50 nm and corresponding to the charge-storage capacitance Cst (m, n), and formed on the poly-Si film **30** through a gate insulating film **20** formed from SiO_2 are gate wiring electrodes **14** of the EL drive TFTs composed of Mo.

[0138] Anode current feeding wiring electrodes An are formed on the gate wiring electrodes **14** of the EL drive TFTs through an interlayer insulating film **21** composed of SiO_2, and are of a three-layered electrode structure composed of Mo (**110***a*), Al (**110***b*), and Mo (**110***c*).

[0139] Here, the gate wiring electrode **14** of the EL drive TFT (Qd**3**(*m, n*)) shown in FIG. **7** is shown as its portion being extended below the anode current feeding wiring electrode An such that the gate wiring electrode **14** of the EL drive TFT (Qd**3** (*m, n*)) overlaps the anode current feeding wiring electrode An as shown in FIG. **5**.

Also, the poly-Si film **30** shown in FIG. **7** is formed to overlap the anode current feeding wiring electrode An as shown in FIG. **5**, and the poly-Si film **30** is electrically connected to the anode current feeding wiring electrode An via a contact hole (CHO in FIG. **5**).

[0140] Accordingly, in the embodiment, the charge-storage capacitance Cst(m, n) is defined by a capacitative element formed by the interlayer insulating film **21** between the anode current feeding wiring electrode An and the gate wiring electrode **14**, and a capacitative element formed by a gate insulating film **20** between the gate wiring electrode **14** and the poly-Si film **30**.

[0141] In this manner, pixels are improved in numerical aperture by forming the charge-storage capacitance Cst(m, n) below the anode current feeding wiring electrode An.

[0142] Also, picture signal wiring electrodes (Dn, D(n+1)) are also formed on the same layer as the anode current feeding wiring electrode An, and the picture signal wiring electrodes (Dn, D(n+1)) are of a three-layered electrode structure composed of Mo (**11***a*), Al (**11***b*), and Mo (**11***c*).

[0143] All these constituents are covered by a protective insulating film **22** having a film thickness of 200 nm and composed of Si_3N_4, on which film is formed an anode electrode **13** composed of an indium-tin oxide (ITO).

Further, an organic insulating film **23** having a film thickness of 2 μm and containing polyimide as its main component is formed on the anode electrode **13**, and the organic insulating film **23** is provided substantially centrally of the anode electrode **13** with an opening.

[0144] Formed on the anode electrode **13** and the organic insulating film **23** is an electron hole transport layer **300** having a film thickness of 150 nm and composed of triphenyldiamine (TPD), and formed on the layer are a red EL luminescent layer **301**R composed of a tris (8-hydroxyquinoline) aluminum (Alq3) having a film thickness of 30 nm and doped with DCJTB and rubrene, and an electron transport layer (not shown) having a film thickness of 30 nm and composed of Alq3.

[0145] Formed above the electron transport layer through LiF having a film thickness of 0.8 nm is a cathode electrode **302** having a film thickness of 150 nm.

[0146] Electron holes injected from the anode electrode **13** and electrons injected from the cathode electrode **302** make radiational reunion in the red EL luminescent layer **301**R to cause emission.

Light generated is emitted toward the glass substrate **1**.

[0147] Arranged in adjacent pixels are blue dots and green dots, on which a blue EL luminescent layer **301**B and a green EL luminescent layer **301**G are formed in place of a red EL luminescent layer.

[0148] The blue EL luminescent layer **301**B is DPVBi doped with BCzVBi having a film thickness of 15 nm, and the green EL luminescent layer **301**G is Alq3 doped with coumarin **540** having a film thickness of 30 nm.

[0149] FIG. **8** is a cross sectional view showing a cross-sectional structure cut along the cut line Y-Y' shown in FIG. **5**, and FIG. **9** is a cross sectional view showing a cross-sectional structure cut along the cut line Z-Z' shown in FIG. **5**.

[0150] As described above, the buffer Si_3N_4 film **200** having a thickness of 50 nm and the buffer SiO_2 film **2** having a thickness of 100 nm are formed on the non-alkali glass substrate **1**, the poly-Si film **30** having a thickness of 50 nm and corresponding to the switch TFT (Qs(m,n)) and the EL drive TFT (Qd**2**(*m, n*)) is formed on the films, and the scanning signal wiring electrodes Gm and the gate wiring electrodes **14** of the EL drive TFTs are formed on the poly-Si film **30** through the gate insulating film **20** formed from SiO_2.

Here, the scanning signal wiring electrodes Gm are formed from Mo.

[0151] The switch TFT (Qs(m,n)) is composed of a N type TFT, the picture signal wiring electrode Dn is connected to a source electrode of the switch TFT through a contact hole opened to the interlayer insulating film **21**, and the connection wiring electrode **12** is connected to a drain electrode of the switch TFT.

[0152] As described above, the picture signal wiring electrode Dn is of a three-layered electrode structure composed of Mo (**11***a*), Al (**11***b*), and Mo (**11***c*), and likewise the connection wiring electrodes **12** are of a three-layered electrode structure composed of Mo (**12***a*), Al (**12***b*), and Mo (**12***c*).

[0153] The other of the connection wiring electrodes **12** is also connected to the gate wiring electrodes **14** of the EL drive TFTs via through holes formed in the interlayer insulating film **21**, so that a signal voltage of the picture signal wiring electrode Dn is applied to the gate wiring electrode **14** of the EL drive TFT via the switch TFT (Qs(m,n)).

[0154] Meanwhile, the EL drive TFT (Qd**2**(*m, n*)) is composed of a P type TFT, to a source electrode of which the anode current feeding wiring electrode An is connected via a contact hole opened to the interlayer insulating film **21**.

[0155] As described above, the anode current feeding wiring electrode An is of a three-layered electrode structure composed of Mo (**110***a*), Al (**110***b*), and Mo (**110***c*).

[0156] A drain electrode of the EL drive TFT (Qd**2**(*m, n*)) is made common to drain electrodes of the EL drive TFT (Qd**1** (*m,n*−1)) and the EL drive TFT (Qd**3**(*m,n*+1)), which are adjacent to the EL drive TFT (Qd**2**(*m, n*)), to be connected to the EL connection wiring electrode **15**.

[0157] Here, the EL connection wiring electrodes **15** are of a three-layered electrode structure composed of Mo (**15***a*), Al (**15***b*), and Mo (**15***c*).

[0158] Also, the anode electrodes **13** are connected to the EL connection wiring electrodes **15** via through holes formed in the protective insulating film **22** having a film thickness of 200 nm and composed of Si_3N_4.

Organic LEDs having the above layered structure are formed above the anode electrodes **13**.

Third Embodiment

[0159] FIG. **10** is a circuit diagram showing equivalent networks for pixels in a display device according to a third embodiment of the invention, and FIG. **11** is a plan view showing a pixel arrangement in the display device according to the third embodiment of the invention.

[0160] With the self-luminescence display device according to the embodiment, an EL element OLED(m, n) in row m and column n is driven by five parallel EL drive TFTs formed in total five regions of pixels in row m and column (n−2), row m and column (n−1), row m and column (n+1), and row m and column (n+2) as well as in row m and column n.

[0161] Since the number in parallel is five, such averaging greatly contributes to improvement in uniformity, which makes it possible to obtain an enhanced uniform display characteristics.

Fourth Embodiment

[0162] FIG. **12** is a circuit diagram showing equivalent networks for pixels in a display device according to a fourth embodiment of the invention, and FIG. **13** is a plan view showing a pixel arrangement in the display device according to the fourth embodiment of the invention.

[0163] With the self-luminescence display device according to the embodiment, an EL element OLED(m, n) in row m and column n is driven by six parallel EL drive TFTs formed in total six regions of pixels in row m and column (n+1), row m and column (n+2), row m and column (n+3), row m and column (n+4), and row m and column (n+5) as well as in row m and column n.

[0164] Since the number in parallel is six, such averaging greatly contributes to improvement in uniformity, which makes it possible to obtain an enhanced uniform display characteristics.

[0165] Also, the embodiment adopts a configuration, in which light emitted from the EL elements is taken not from a side of the substrate but a side of a front surface.

[0166] When the number of TFTs in pixels is increased as in the embodiment, it becomes difficult to ensure an area of those EL elements, which contribute to emission of light.

[0167] In such case, that configuration, in which light is taken from the side of a front surface, is advantageous.

[0168] FIG. **14** is a cross sectional view showing a cross-sectional structure cut along the line X-X' shown in FIG. **13**. As shown in FIG. **14**, a buffer Si_3N_4 film **200** having a thickness of 50 nm and a buffer SiO_2 film **2** having a thickness of 100 nm are formed on a non-alkali glass substrate **1** having a thickness of 0.5 mm and a strain temperature of about 670° C.

[0169] Formed on the buffer SiO_2 film **2** is a polycrystal Si film **30** having a thickness of 50 nm and corresponding to the charge-storage capacitance Cst(m, n), and formed on the poly-Si film **30** through a gate insulating film **20** formed from SiO_2 are gate wiring electrodes **14** of the EL drive TFTs composed of Mo.

[0170] The gate wiring electrode **14** of the EL drive TFT (Qd**3**(*m, n*)) shown in FIG. **14** is shown as its portion being extended below an associated pixel as shown in FIG. **13**, and the poly-Si film **30** shown in FIG. **14** is electrically connected to the anode current feeding wiring electrode An through the contact hole as shown in FIG. **13**.

[0171] The anode current feeding wiring electrode An is formed above the gate wiring electrode **14** of the EL drive TFT with an interlayer insulating film **21** formed from SiO_2 therebetween. The anode current feeding wiring electrode An is of a three-layered electrode structure composed of Mo (**110***a*), Al (**110***b*), and Mo (**110***c*).

[0172] Also, a picture signal wiring electrode Dn and a reflective film **17** are also formed on the same layer as the anode current feeding wiring electrode An.

The picture signal wiring electrode Dn is of a three-layered electrode structure composed of Mo (**11***a*), Al (**11***b*), and Mo (**11***c*), and the reflective film **17** is also of a three-layered electrode structure composed of Mo/Al/Mo.

[0173] The reflective film **17** is connected to an anode electrode **13** via openings (CH**1**, Cf**2** in FIG. **13**) formed in a protective insulating film **22** having a film thickness of 200 nm and composed of Si_3N_4.

The reflective film **17** is formed in a region in, for example, a pixel in row m and column n, except for that region, in which a switch TFT and an EL drive TFT (Qd**1**(*m,n*)) are formed.

[0174] The reflective film **17** serves to reflect light emitted from an EL element to a front surface and constitutes a part of the charge-storage capacitance Cst(m, n) between it and the poly-Si film **30** when the EL drive TFT (Qd**3**(*m, n*)) is ON.

[0175] Accordingly, in the embodiment, the charge-storage capacitance Cst(m, n) is defined by a capacitative element formed by the gate insulating film **20** between the gate wiring electrode **14** and the poly-Si film **30**, and a capacitative element formed by an interlayer insulating film **21** between the reflective film **17** and the poly-Si film **30**.

[0176] All these constituents are covered by a protective insulating film **22** having a film thickness of 200 nm and formed from Si_3N_4, on which film is formed an anode electrode **13** composed of an indium-tin oxide (ITO).

Further, an organic insulating film **23** having a film thickness of 2 μm and containing polyimide as its main component is formed on the anode electrode **13**, and the organic insulating film **23** is provided substantially centrally of the anode electrode **13** with an opening.

[0177] Formed on the anode electrode **13** and the organic insulating film **23** is an electron hole transport layer **300** having a film thickness of 150 nm and composed of triphenyldiamine (TPD), and formed on the layer are a red EL luminescent layer **301**R and composed of a tris (8-hydroxyquinoline) aluminum (Alq3) having a film thickness of 30 nm and doped with DCJTB and rubrene, and an electron hole transport layer (not shown) having a film thickness of 30 nm and composed of Alq3.

[0178] Formed above the electron hole transport layer through LiF having a film thickness of 0.8 nm are 2-9-dimethyl-4, 7diphenyl-1,10-phenanthroline (BCP) having a film thickness of 7 nm and ITO having a film thickness of 77 nm to constitute a transparent cathode electrode **302**.

[0179] Electron holes injected from the anode electrode **13** and electrons injected from the cathode electrode **302** make radiational reunion in the red EL luminescent layer **301**R to cause emission.

Light generated is emitted toward the transparent cathode electrode.

[0180] Arranged in adjacent pixels are blue dots and green dots, on which a blue EL luminescent layer **301**B and a green EL luminescent layer **301**G are formed in place of a red EL luminescent layer.

[0181] The blue EL luminescent layer is DPVBi doped with BCzVBi having a film thickness of 15 nm, and the green EL luminescent layer is Alq3 doped with coumarin **540** having a film thickness of 30 nm.

[0182] FIG. **15** is a graph indicating the relationship between the number N of parallel EL drive TFTs and dispersion (MAX−MIN)/(MAX+MIN) in luminance among pixels.

[0183] As seen from the graph in FIG. **15**, dispersion in luminance in the case of N=3 can be reduced to about a half of that in the case of N=1.

[0184] Theoretically, it is presumed that with respect to the parallel number N, the degree of dispersion is decreased inversely proportional to $\sqrt{N}$.

According to the graph in FIG. **15**, a dispersion decreasing effect as appropriately presumed theoretically is obtained.

Fifth Embodiment

[0185] An entire configuration of the display device according to the invention in a fifth embodiment of the invention will be described below with reference to FIGS. **16** to **18**.

[0186] Formed on the glass substrate **1** are an active matrix AMX constituted by TFTs, a vertical scanning circuit VDRV and a picture signal circuit HDRV.

[0187] The cathode electrode **302** of the EL element OLED is connected to a wiring **401** taken out and formed on the glass substrate **1** through a contact hole in a contact area **400** and then to an external connection terminal PAD.

[0188] Also, all anode current feeding wiring electrodes A provided in respective columns in pixels are connected outside pixel regions to the external connection terminal PAD through a taken-out electrode **402**.

[0189] The embodiment has a feature in that the contact area **400** is arranged between the active matrix AMX and the external connection terminal PAD and the picture signal circuit HDRV is disposed on an opposite side of the active matrix AMX to the external connection terminal PAD.

[0190] With such arrangement, the taken-out wiring **401** extending from the external connection terminal PAD to the contact area **400** can be made short, so that voltage drop and power consumption caused by resistance of the taken-out wiring can be minimized.

[0191] Since current from the EL elements OLED in all pixels flows through the taken-out wiring of the cathode electrode **302**, reduction in resistance of the taken-out wiring is important.

[0192] Meanwhile, since current flowing through a power source wiring and ground wiring to the picture signal circuit HDRV is small as compared with current flowing through the EL elements OLED, no significant problem is caused even when such wirings are lengthened more or less.

[0193] FIG. **17** is an exploded, perspective view showing the entire display device shown in FIG. **16**.

[0194] A seal glass **600** is mounted through a seal SHL on the glass substrate **1**, on which the cathode electrode **302** of the EL elements OLED is formed, whereby the EL elements OLED are not exposed to outside air.

[0195] Used for the seal SHL is an ultraviolet hardening-type resin, in which fiber glass having a diameter of 10 μm is dispersed.

[0196] The seal glass and the glass substrate **1** substantially correspond to each other in external shape at three sides except a side, from which the external connection terminal PAD is taken out, so that the entire panel is made minimum in external dimension.

[0197] FIG. **18** is a cross sectional view showing a cross-sectional structure of the display device shown in FIG. **16**.

[0198] A chemical adsorbent **602** for absorbing moisture entering from outside and a gas emitted from a material, which forms the EL elements OLED, is held on projections provided in the seal glass **600** by means of a tape **601**.

Calcium oxide (CaO) was used as the chemical adsorbent.

[0199] Also, a dry N2 gas, from which moisture is removed up to the dew-point of −78° C., is sealed in a cavity in the seal glass **600**.

Sixth Embodiment

[0200] A manufacturing process, according to a sixth embodiment of the invention, for an active matrix substrate in the display device according to the second embodiment will be described below with reference to FIGS. **19** to **27**.

[0201] First, the plasma CVD method making use of a mixture gas of SiH_4, NH_3 and N_2 is used to form a Si_3N_4 film **200** having a thickness of 50 nm after a non-alkali glass substrate **1** having a thickness of 0.5 mm, a length of 750 mm and a width of 950 mm and a strain temperature of about 670° C. is cleaned.

[0202] Subsequently, the plasma CVD method making use of a mixture gas of tetraethoxysilane and O_2 is used to form a SiO_2 film **2** having a thickness of 120 nm.

In addition, both Si_3N_4 and SiO_2 are formed at temperature of 400° C.

[0203] Then a substantially intrinsic hydro-amorphous silicon film **35** having a thickness of 50 nm is formed on the SiO_2 film **2** by the plasma CVD method making use of a mixture gas of SiH_4 and Ar.

A deposition temperature was 400° C. and an amount of hydrogen was about 5 atomic % immediately after deposition.

[0204] Subsequently, the substrate is annealed at 450° C. for about 30 minutes whereby hydrogen in the hydro-amorphous silicon film **35** is caused to be released.

[0205] Subsequently, the plasma CVD method making use of a mixture gas of tetraethoxysilane and O_2 is used to form a SiO_2 film **201** having a thickness of 100 nm, and then boron (B+) is implanted in a dose 5×10^{12} (atoms/cm^2) at acceleration voltage of 40 KeV by ion-implantation.

Boron serves to adjust a threshold voltage of TFT (see FIG. **19**).

[0206] Subsequently, the SiO_2 film **201** is removed by a buffer hydrofluoric acid, and pulse excimer laser of a wavelength of 308 nm processed in the form of stripe having a short side of 0.3 mm and a long side of 300 mm is irradiated on the amorphous silicon film **35** at a fluence of 450 mJ/cm^2 while moving at 10 μm in a direction along the short side, whereby the amorphous silicon film **35** is melted and recrystallized to provide a P type polycrystal silicon film **30** (see FIG. **20**).

[0207] At this time, dispersion in the TFT characteristics caused by dispersion in crystal quality of the polycrystal silicon in a scanning direction of laser beam generally tends to become greater than dispersion in a direction perpendicular to the scanning direction of laser beam.

[0208] Therefore, a great effect is obtained by arranging a plurality of EL drive TFTs in parallel in the scanning direction of laser beam.

[0209] The scanning direction of laser beam shown by arrows in FIG. **3** or **6** indicates this, and the plurality of EL

drive TFTs are arranged substantially in parallel in the scanning direction of laser beam.

The same is with the embodiment shown in FIGS. **10** and **12**.

[0210] Subsequently, the reactive ion etching method making use of CF_4 is used to process the P type polycrystal silicon film **30** in a predetermined form to obtain TFTs and a wiring pattern (P type polycrystal silicon film **30**) except the TFTs.

[0211] Subsequently, the plasma CVD method making use of a mixture gas of tetraethoxysilane and O_2 is used to form SiO_2 having a thickness of 100 nm to form a gate insulating film **20**.

[0212] Subsequently, after the sputtering method is used to form a Mo film having a thickness of 200 nm, an ordinary photolithography method is used to form a predetermined resist pattern PR on the Mo film, and the reactive ion etching method making use of CF_4 is used to process the Mo film in a predetermined form to obtain gate electrodes **10**N for N type TFTs.

[0213] Subsequently, while the resist pattern PR used in etching is left, phosphorus (P) ions are implanted in a dose 10^{15} (atoms/cm^2) at acceleration voltage of 60 KeV by ion-implantation to form regions of source electrodes and drain electrodes for N type TFTs (see rightward and central portions in FIG. **21**).

[0214] At this time, all the elements are protected by patterns of the Mo film and the photoresist film PR to prevent phosphorus ions from being implanted into the P type TFTs (see a leftward portion in FIG. **21**).

[0215] Subsequently, while the resist pattern is left, the substrate is processed by a mixed acid and the Mo electrodes thus processed are subjected to side etching whereby the pattern is slimmed and the resist is removed, after which P ions are implanted in a dose 2×10^{13}(atoms/cm^2) at acceleration voltage of 65 KeV by ion-implantation to form LDD regions for N type TFTs.

The LDD regions are controlled in length by a side etching time with the mixed acid (see FIG. **22**).

[0216] Subsequently, a predetermined resist pattern is formed on the Mo film, and the reactive ion etching method making use of CF_4 is used to obtain gate electrodes **10**P for P type TFTs and a wiring pattern (gate wiring electrode **14**) except the TFTs.

[0217] Using the gate electrodes **10**P for P type TFTs as a mask, boron ions are implanted in a dose 10^{15} (atoms/cm^2) at acceleration voltage of 40 KeV by ion-implantation to form regions of source electrodes and drain electrodes for P type TFTs.

At this time, all N type TFTs are protected by the photoresist pattern PR to be protected from the etching gas and prevent boron ions from being implanted thereinto (see FIG. **23**).

[0218] After the photoresist is removed, ultraviolet light from an excimer lamp or metal halide lamp is irradiated to activate impurities implanted by the rapid thermal anneal (RTA) method (see FIG. **24**).

[0219] Subsequently, the plasma CVD method making use of a mixture gas of tetraethoxysilane and oxygen is used to form SiO_2 having a film thickness of 500 nm to form an interlayer insulating film **21**.

[0220] After a predetermined resist pattern is formed, the wet etching method making use of a mixed acid is used to form contact through holes in the interlayer insulating film **21**.

[0221] Subsequently, after the sputtering method is used to sequentially laminate Mo film of 50 nm, an Al—Nd alloy of 500 nm and Mo of 50 nm, a predetermined resist pattern is formed, and then the reactive ion etching method making use of a mixed gas of BCl_3 and Cl_2 performs etching collectively to fabricate picture signal wiring electrodes D, anode current feeding wiring electrodes A, connection wiring electrodes **12** and EL connection wiring electrodes **15** (see FIG. **25**).

[0222] Subsequently, the plasma CVD method making use of a mixture gas of SiH_4, NH_3 and N_2 is used to form a Si_3N_4 film having a thickness of 400 nm to make the same a protective insulating film **22**.

[0223] After a predetermined photoresist pattern is formed, the dry etching method making use of SF_6 is used to form contact through holes in the protective insulating film **22**.

[0224] Succeedingly, the sputtering method is used to form an ITO film of 70 nm and the wet etching method making use of a mixed acid is used to process the film in a predetermined shape to form anode electrode **13** for EL elements OLED (see FIG. **26**).

[0225] Finally, the spin coating method is used to coat a photosensitive polyimide resin in a film thickness of about 3.5 μm, and a predetermined mask is used to perform exposure and development to remove the polyimide resin in those portions of the anode electrode, on which EL elements OLED are formed, thereafter performing baking the polyimide resin for 30 minutes at 350° C. to form an organic insulating film **23** having a film thickness of 2.3 μm (see FIG. **27**).

[0226] The organic insulating film **23** is formed to cover ends of the anode electrode **13** to prevent the EL elements OLED from being broken by field concentration at ends of the ITO electrodes when a very thin organic film forming the EL elements OLED is formed on the anode electrode.

[0227] A process of forming EL elements on an active matrix substrate fabricated by the above processes will be described below.

[0228] The active matrix substrate is set in a vacuum deposition device, and first introduced into a preheating chamber to be baked under vacuum for one hour at 200° C., whereby moisture adsorbing to surfaces of the substrate and moisture contained in the organic insulating film **23** are removed.

[0229] Subsequently, ultraviolet light is irradiated at the intensity of 60 mW/cm^2 for 60 seconds in an atmosphere containing oxygen to remove organic substances on the surfaces of the anode electrode.

[0230] Subsequently, the active matrix substrate is moved into a pretreatment chamber to be subjected to O_2 plasma processing whereby the surfaces of the anode electrode are adjusted in work function.

The processing condition involves 60 seconds at the RF power of 200 W.

[0231] This processing adjusts the work function of ITOs being the anode electrode **13** at 5.1 to 5.2 eV, and decreases a barrier level when electrons are injected into an electron hole transport material, whereby an efficiency of injection can be enhanced.

[0232] Subsequently, the active matrix substrate is moved into a first deposition chamber to be subjected to mask deposition with a mask, in which an electron hole transport layer is formed on an entire display surface.

[0233] Triphenyldiamine (TPD) is used for a material of the electron hole transport layer.

Besides this, for example, α-NPD can be used.

The electron hole transport layer has a film thickness of 150 nm.

[0234] Subsequently, the active matrix substrate is moved into a second deposition chamber to be subjected to mask deposition of luminescent materials for respective RGBs.

[0235] In deposition of different luminescent materials, predetermined materials are formed in dot positions of respective RGBs by first making register between dots representative of blue color and openings in a deposition mask, forming a blue material, shifting the deposition mask a pitch of one dot within the deposition chamber, making deposition of a green material, and further moving the deposition mask similarly to make deposition of a red material.

[0236] Subsequently, the active matrix substrate is moved into a third deposition chamber to form a cathode electrode **302**.

[0237] In order to enhance an efficiency of electron injection for the organic layer, the cathode electrode **302** is formed such that after LiF is formed to have a film thickness of around 0.8 nm, Al is formed to have a thickness of 150 nm.

[0238] Subsequently, the active matrix substrate is moved into a seal chamber, a seal glass having been beforehand baked like the active matrix substrate for dehydration is bonded to the active matrix substrate with an ultraviolet hardening-type resin therebetween, and ultraviolet light is irradiated on a back surface of the active matrix substrate to cure the resin. At this time, a chemical adsorbent is inserted into an air gap in the seal glass.

[0239] All the preceding steps after setting of the active matrix substrate must be effected in a state, in which the active matrix substrate is not exposed to the atmospheric air.

[0240] Finally, the active matrix substrate, to which the seal glass is bonded, is taken out to be cut into a predetermined size, and driver LSIs are loaded on the substrate to finish a panel.

[0241] While the invention having been thought of by the inventors of this application has been concretely described on the basis of the embodiments, it is not limited to the embodiments but can be of course modified within a scope not departing from the gist thereof.

[0242] Effects obtained by typical configurations of the invention disclosed in this application are simply described below.

(1) It is possible in a self-luminescence display device according to the invention to obtain a uniform display screen free of unevenness.

(2) It is possible in a self-luminescence display device according to the invention to reduce voltage drop and power consumption caused by resistance of the taken-out wiring of the cathode electrodes.

What is claimed is:

1. A display device comprising:
a first line;
an organic EL device;
a transistor for controlling current between the first line and the organic EL device,
a second line; and
a capacitor arranged between the second line and a gate of the transistor;
the organic EL device comprising a first electrode, an organic EL layer and a second electrode;
wherein the transistor is covered by a first insulating layer,
wherein the transistor is connected to a connecting line via a first contact hole in the first insulating layer, the connecting line comprising three metal layers, wherein the connecting line is covered by a second insulating layer, and wherein the connecting line is connected to the first electrode via a second contact hole in the second insulating layer,
wherein the first contact hole is deviated from the second contact hole,
wherein the first contact hole, the second contact hole and the connecting line are covered by a third insulating layer, wherein the third insulating layer is arranged on the first electrode, and wherein the third insulating layer includes an aperture on the first electrode, and
wherein the organic EL device is arranged in the aperture.

2. The display device according to claim **1**,
the connecting line comprising a first layer, a second layer and a third layer,
the second layer comprising Al, and
the first layer and the layer comprising Mo.

3. The display device according to claim **2**,
the first line comprising the same layers as the connecting line.

4. The display device according to claim **2**,
the second line comprising the same layers as the connecting line.

5. The display device according to claim **3**,
wherein the first line, the second line and the connecting line are arranged on the same layer.

6. A display device comprising:
a first line;
an organic EL device;
a transistor controlling current between the first line and the organic EL device;
a second line; and
a capacitor connected between the second line and the transistor;
an organic EL device comprising a first electrode, an organic EL layer and a second electrode;
wherein the transistor is covered by a first insulating layer,
wherein a current is supplied from the transistor to the first electrode via a first contact hole in the first insulating layer,
wherein an outer edge of the first electrode is covered by a second insulating layer including an aperture exposing the first electrode,
wherein the first line is arranged under the first electrode covered by the second insulating layer,
wherein a reflective layer is arranged under the first electrode, an outer edge of the reflective layer is covered by the second insulating layer, and the reflective layer is smaller than the first electrode and larger than the aperture of the second insulating layer.

7. The display device according to claim **6**,
wherein a gap is arranged between the reflective layer and the first line.

* * * * *

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摘要(译)

一种自发光显示装置，其中由驱动薄膜晶体管之间的特性分散引起的多个像素之间的显示分散减小，并且可以获得没有不均匀性的均匀显示。该装置包括具有电流驱动型发光元件的多个像素，以及并联连接的n（n≥2）个薄膜晶体管，以将驱动电流馈送到相应的电流驱动型发光元件。晶体管分别布置在不同的像素中，例如，沿第一方向彼此相邻的第一像素区域中。可以沿着所述第一方向在所述第一区域的至少一侧上提供虚设像素的第二区域。